

FIG. 1

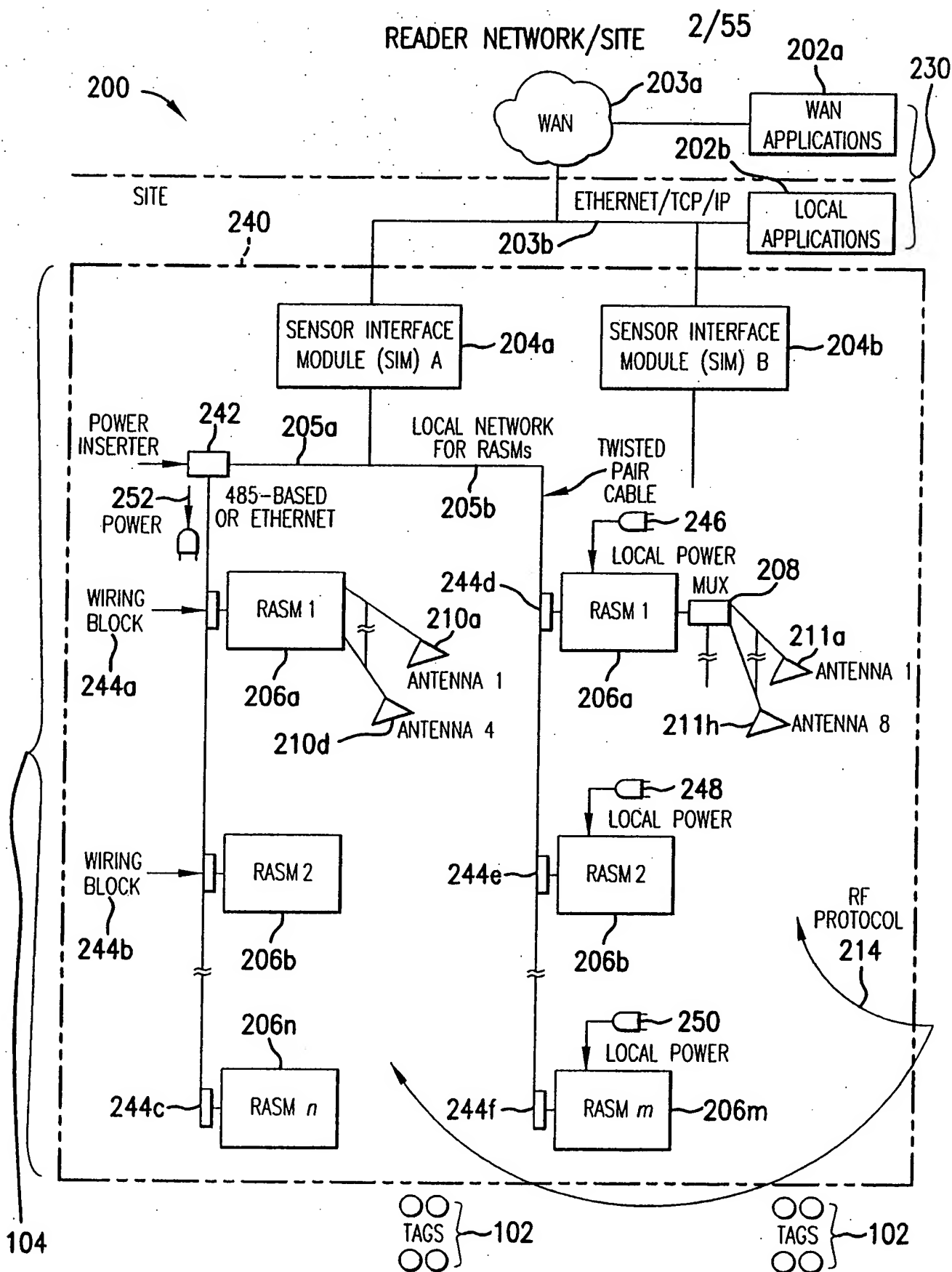


FIG. 2

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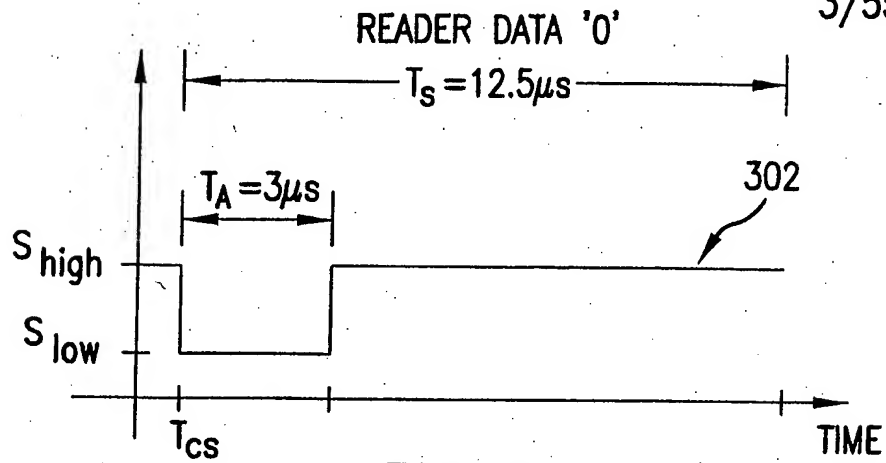


FIG. 3

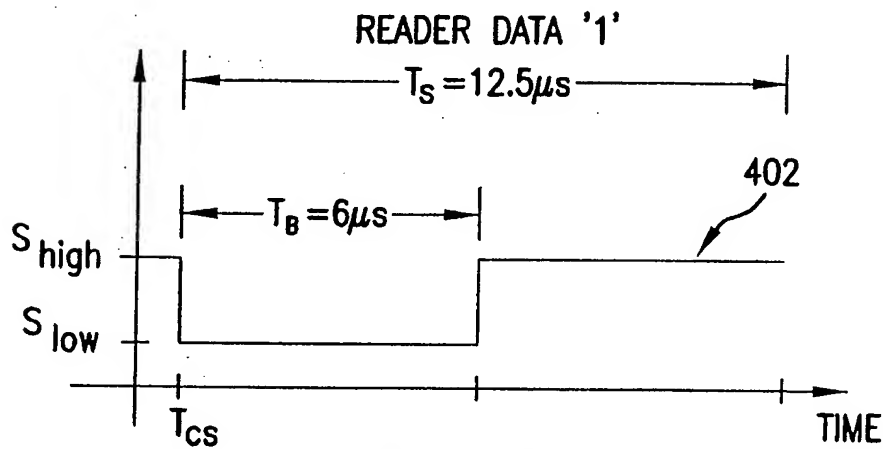


FIG. 4

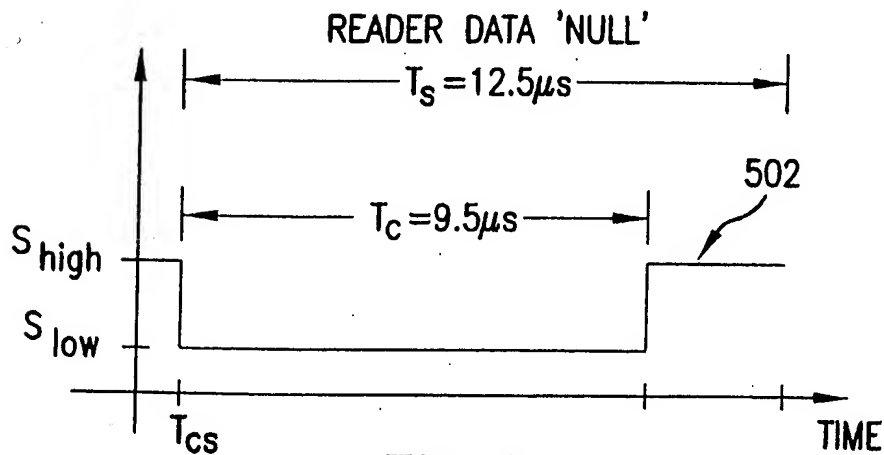


FIG. 5

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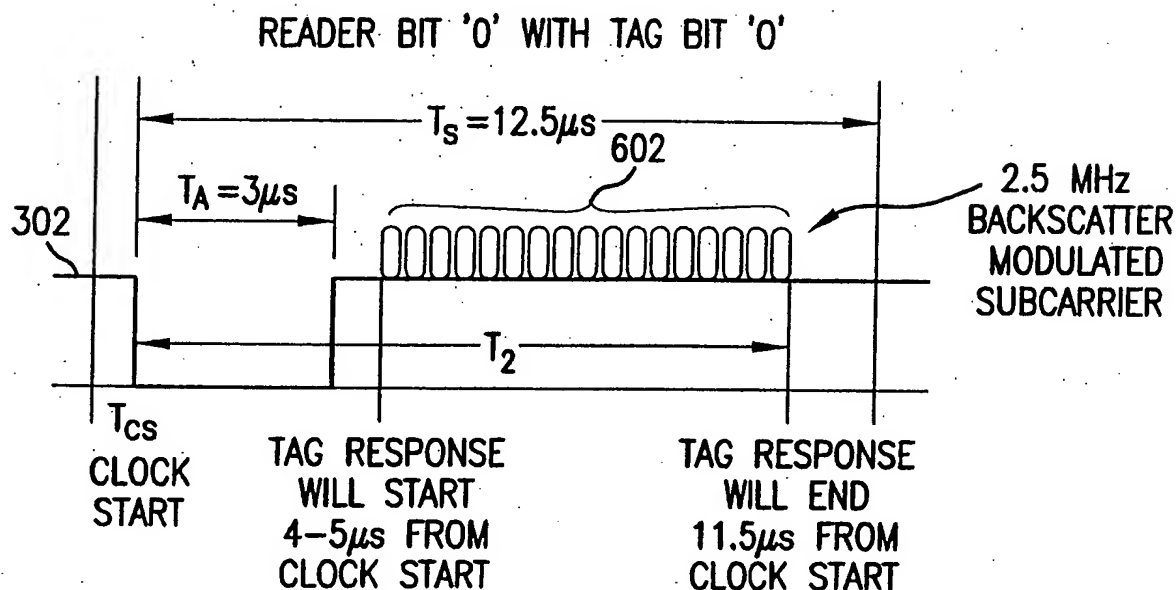


FIG. 6

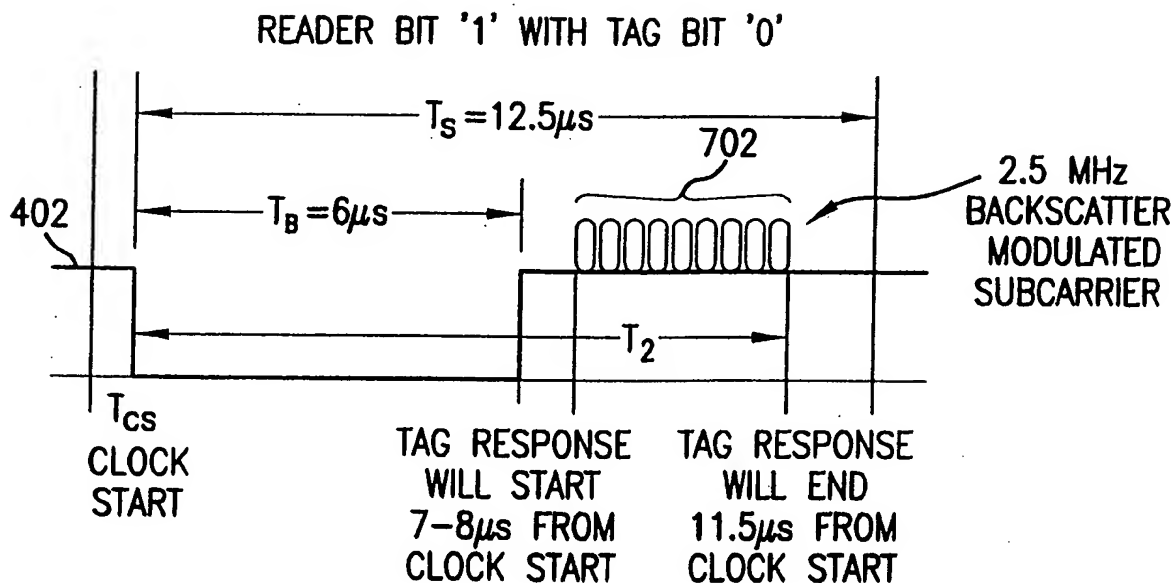


FIG. 7

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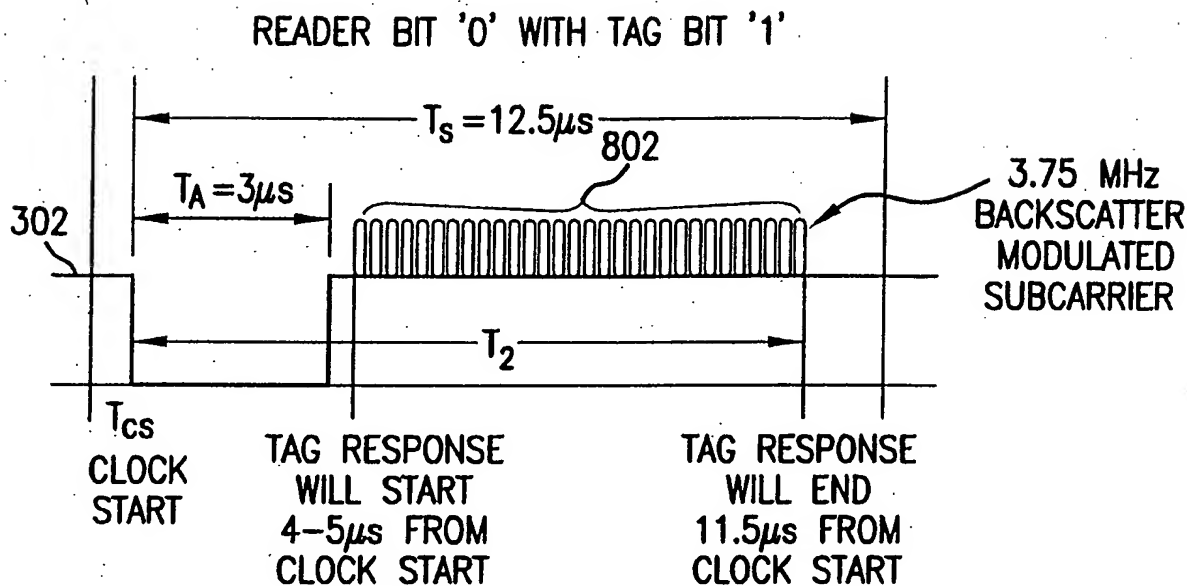


FIG. 8

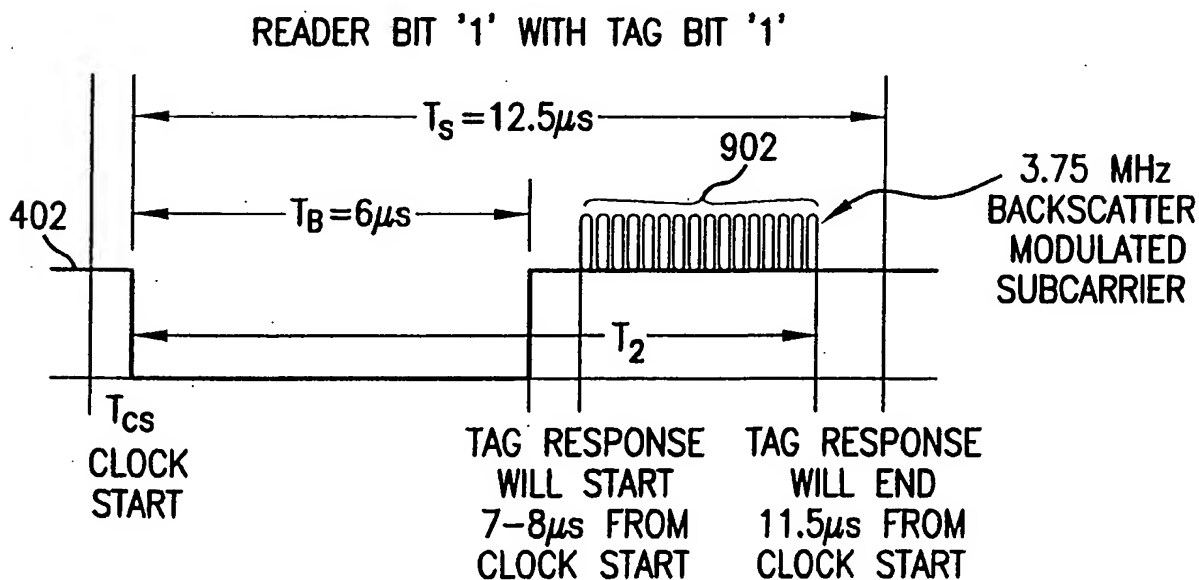


FIG. 9

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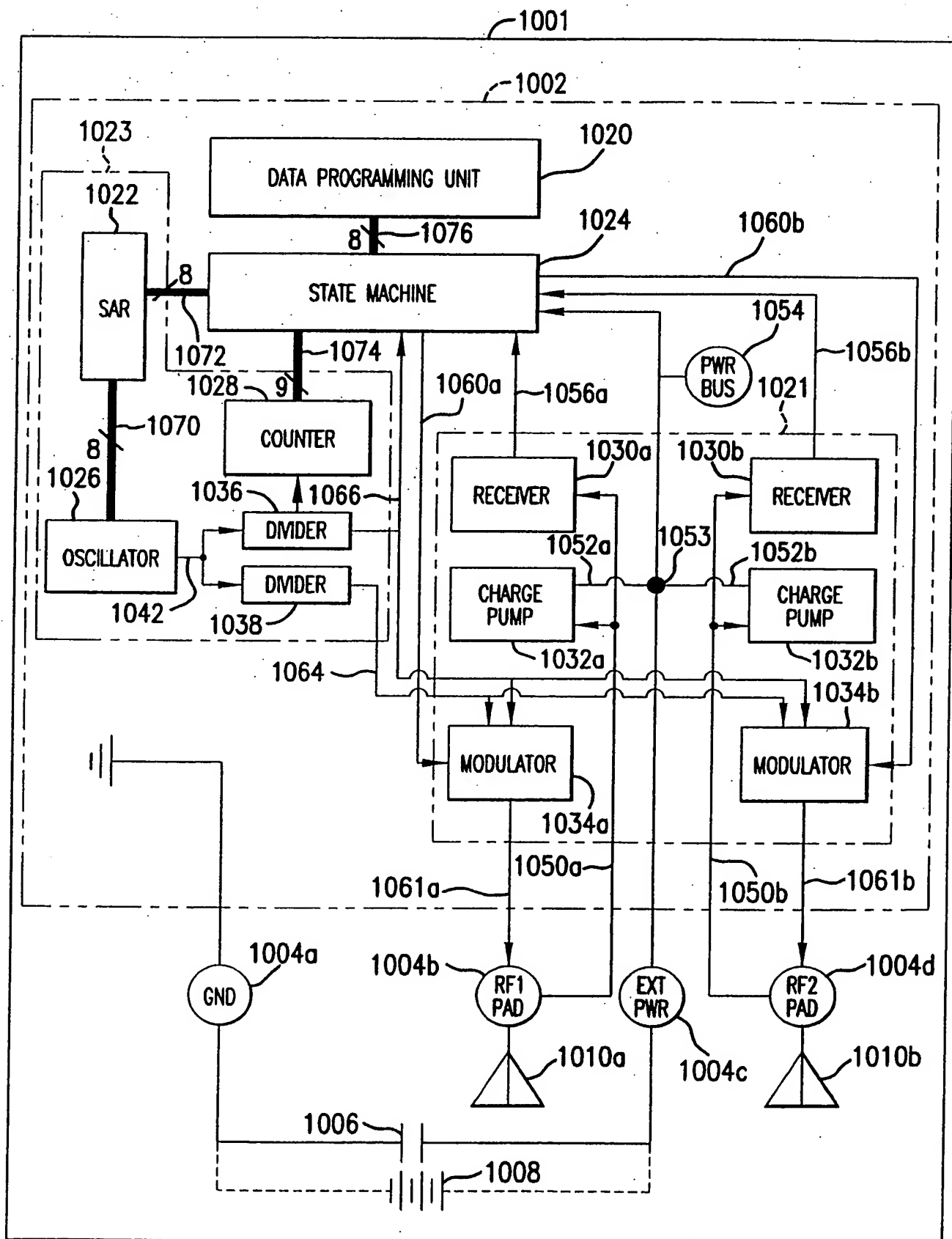


FIG. 10

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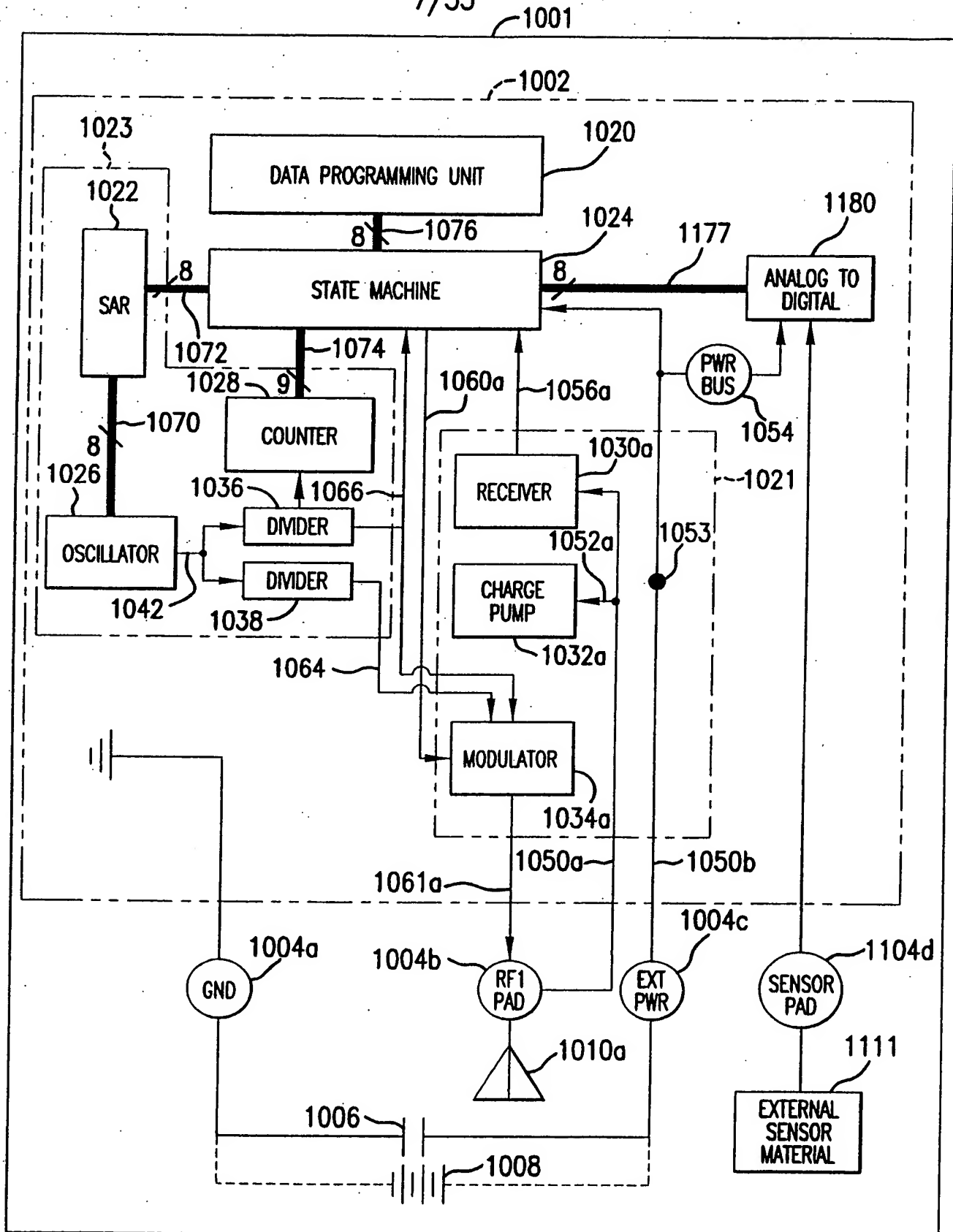


FIG. 11

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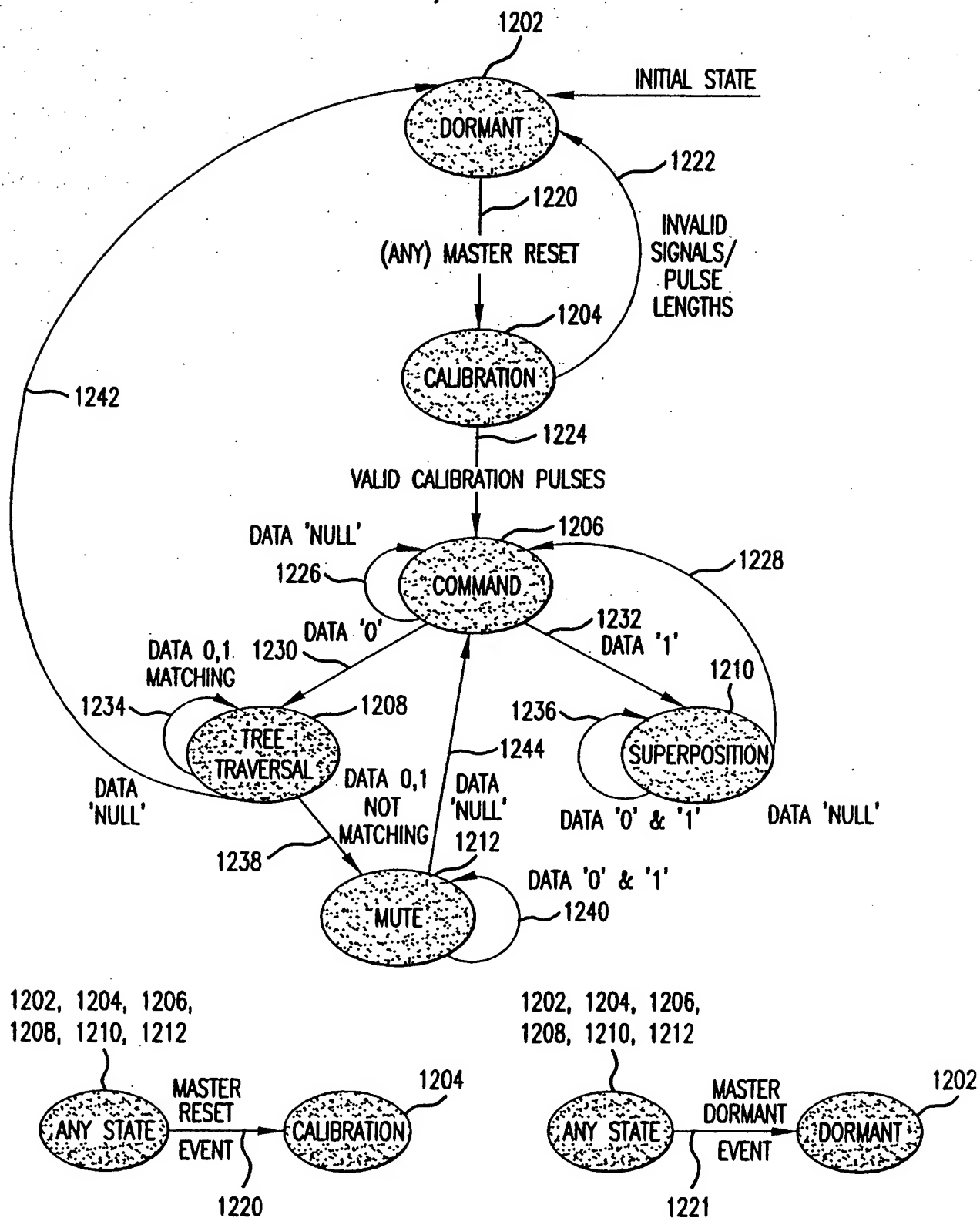


FIG. 12A

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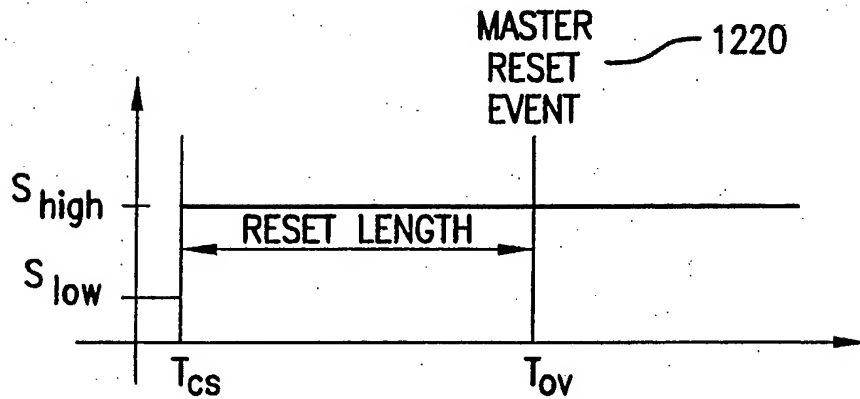


FIG. 12B

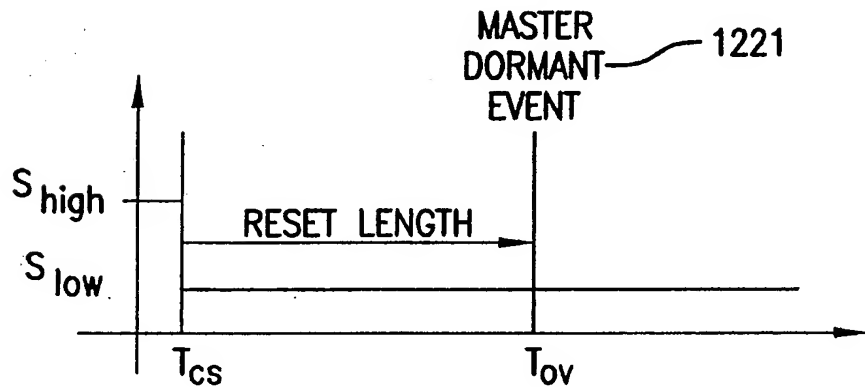


FIG. 12C

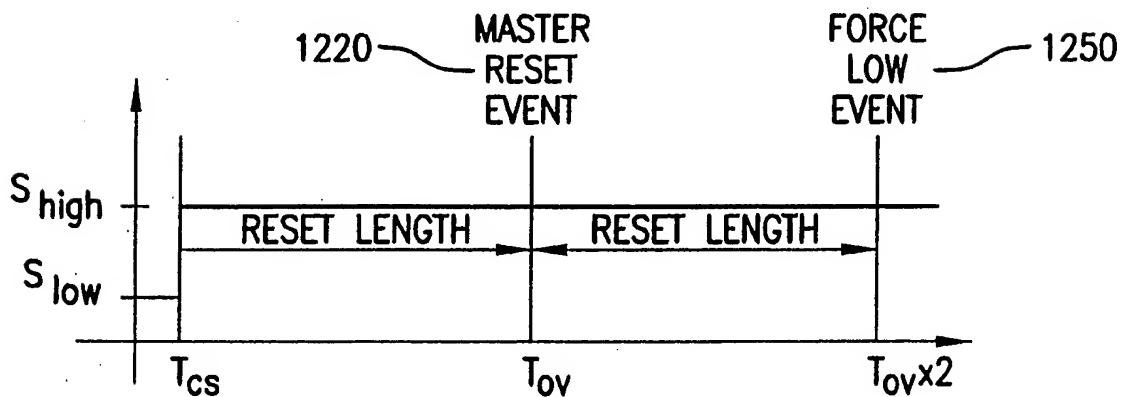
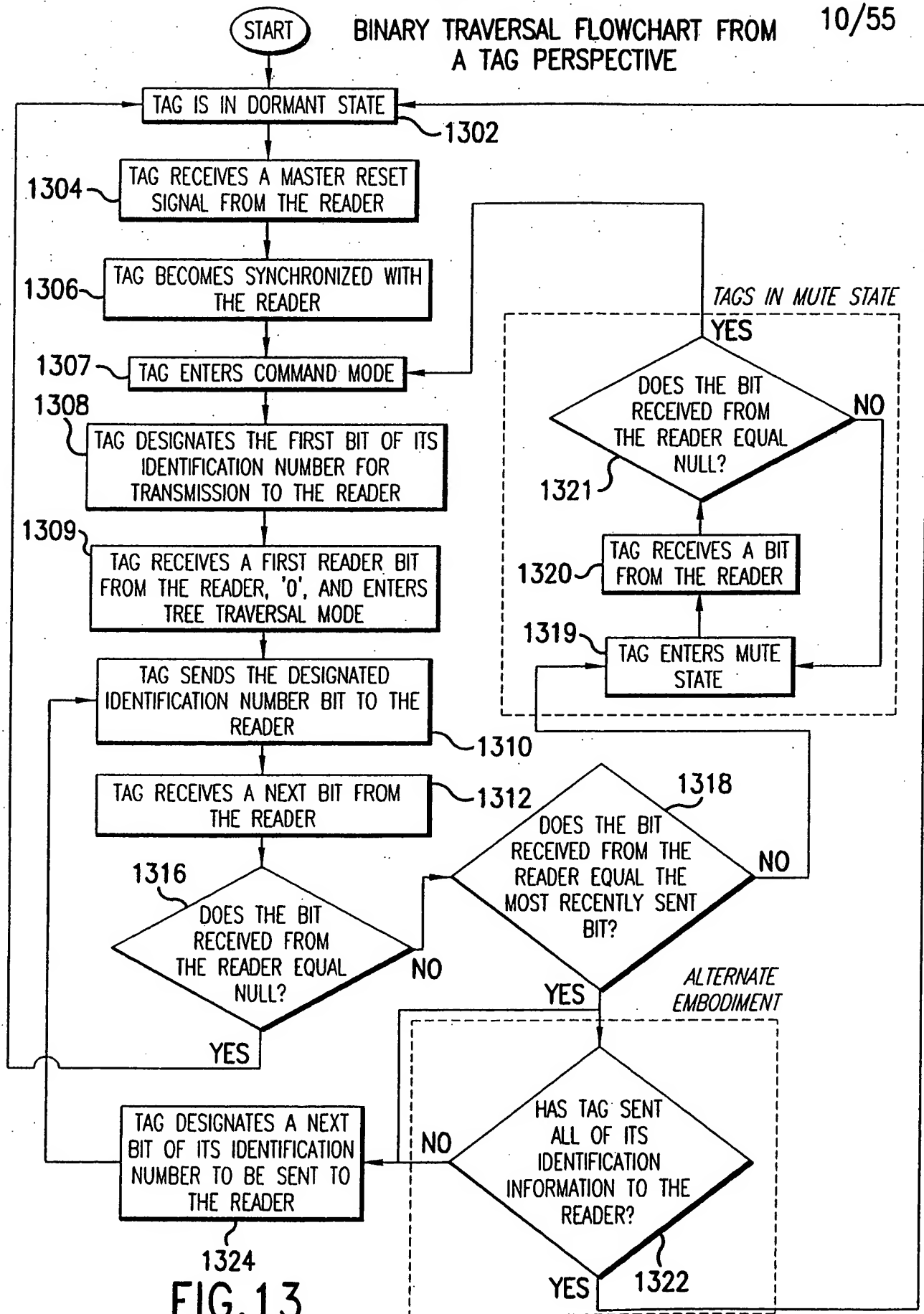


FIG. 12D

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READ SPECIFIC TAG, READER PERSPECTIVE

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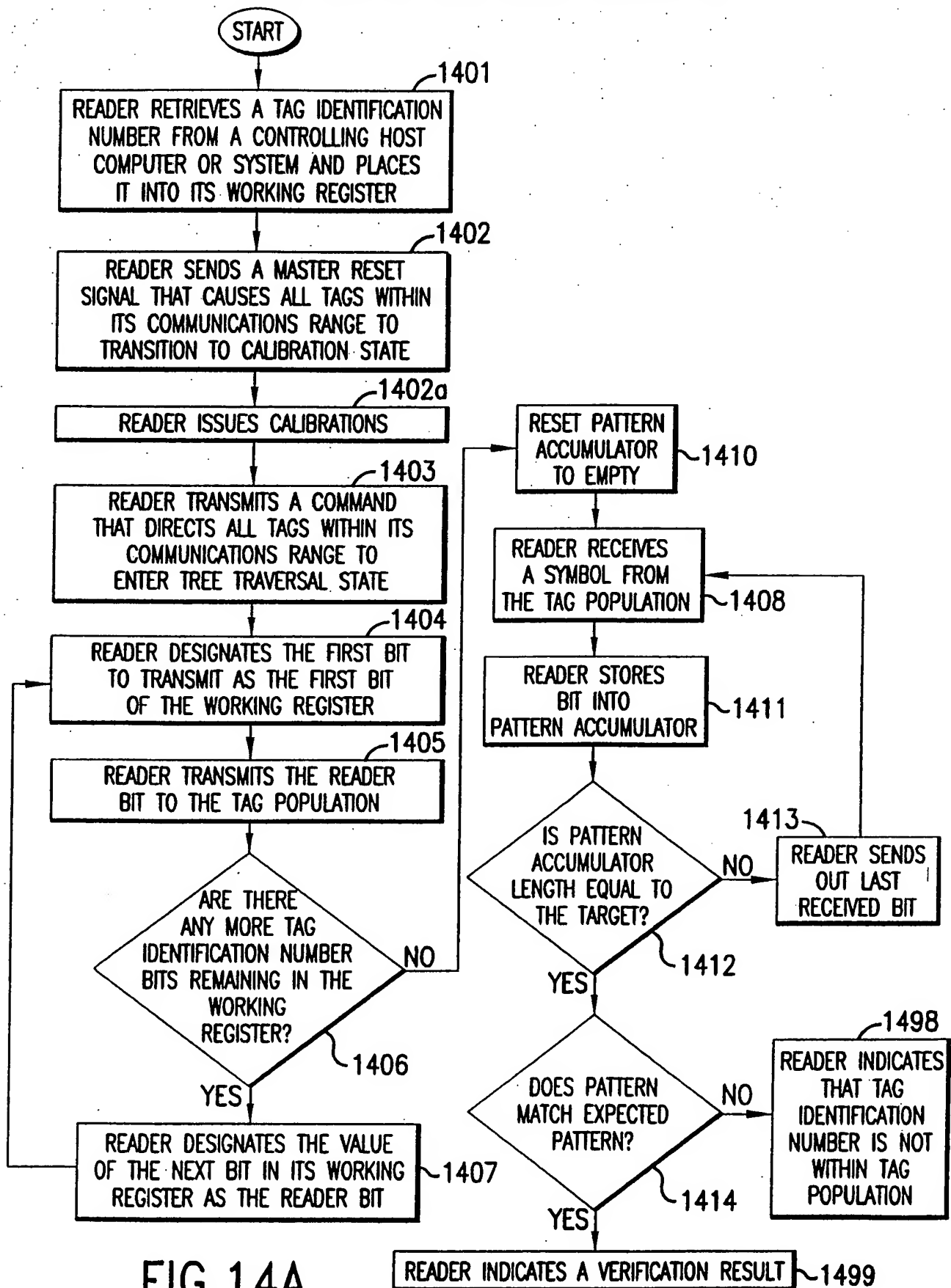


FIG.14A

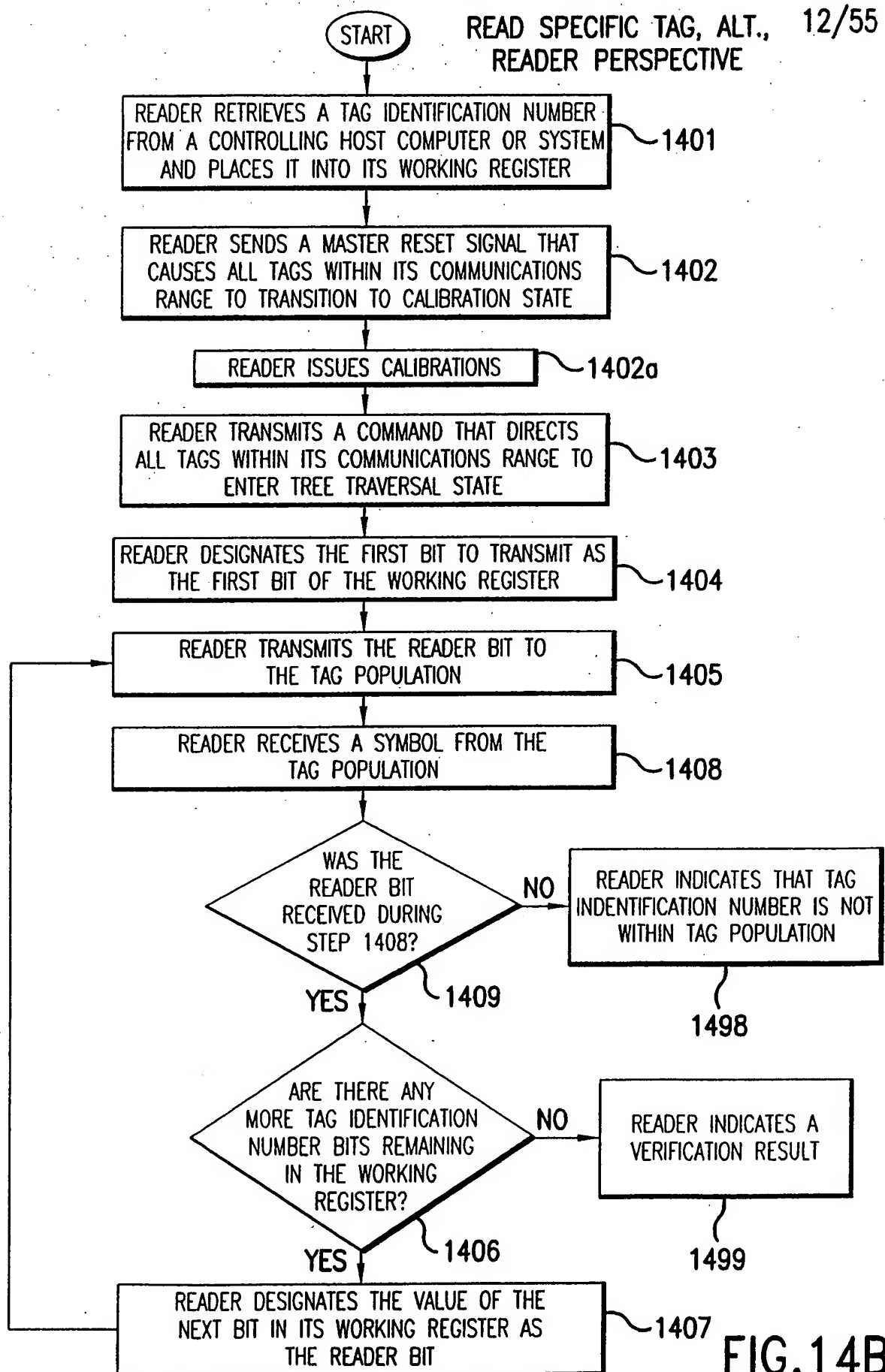


FIG. 14B

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READ ALL TAGS, READER PERSPECTIVES

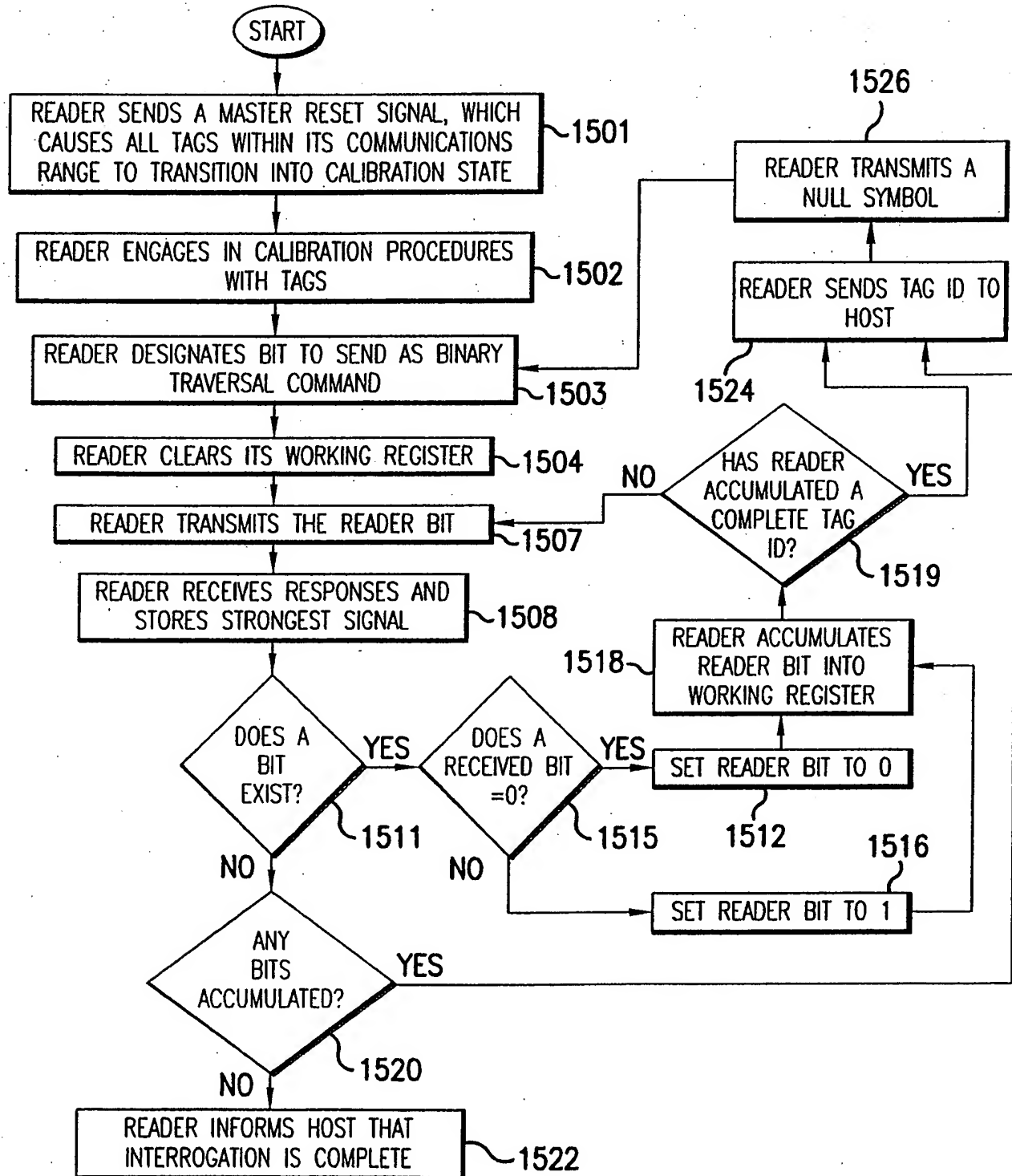


FIG.15A

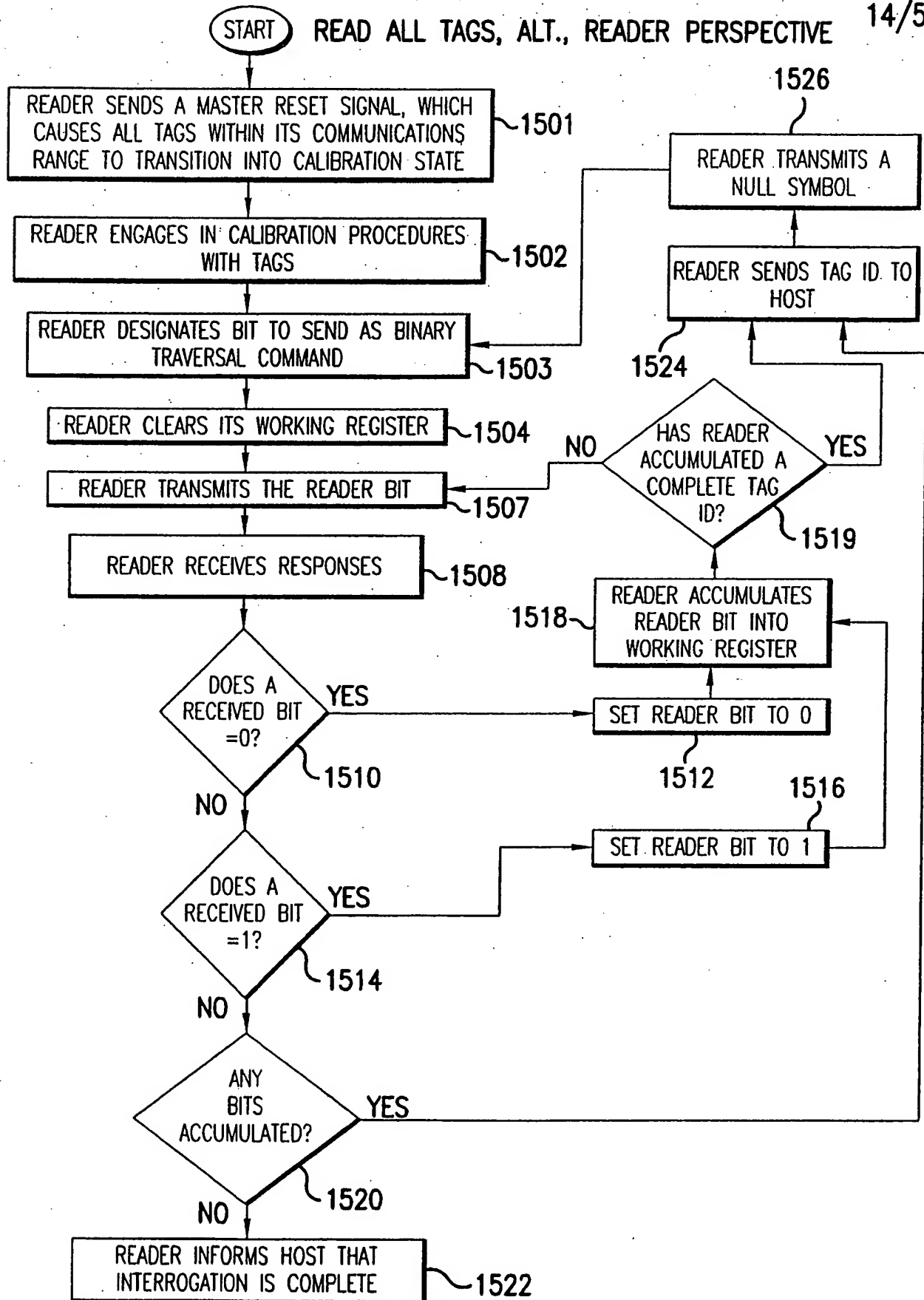


FIG.15B

BINARY TRAVERAL PATHS AND TREE FOR A 3-BIT TAG POPULATION

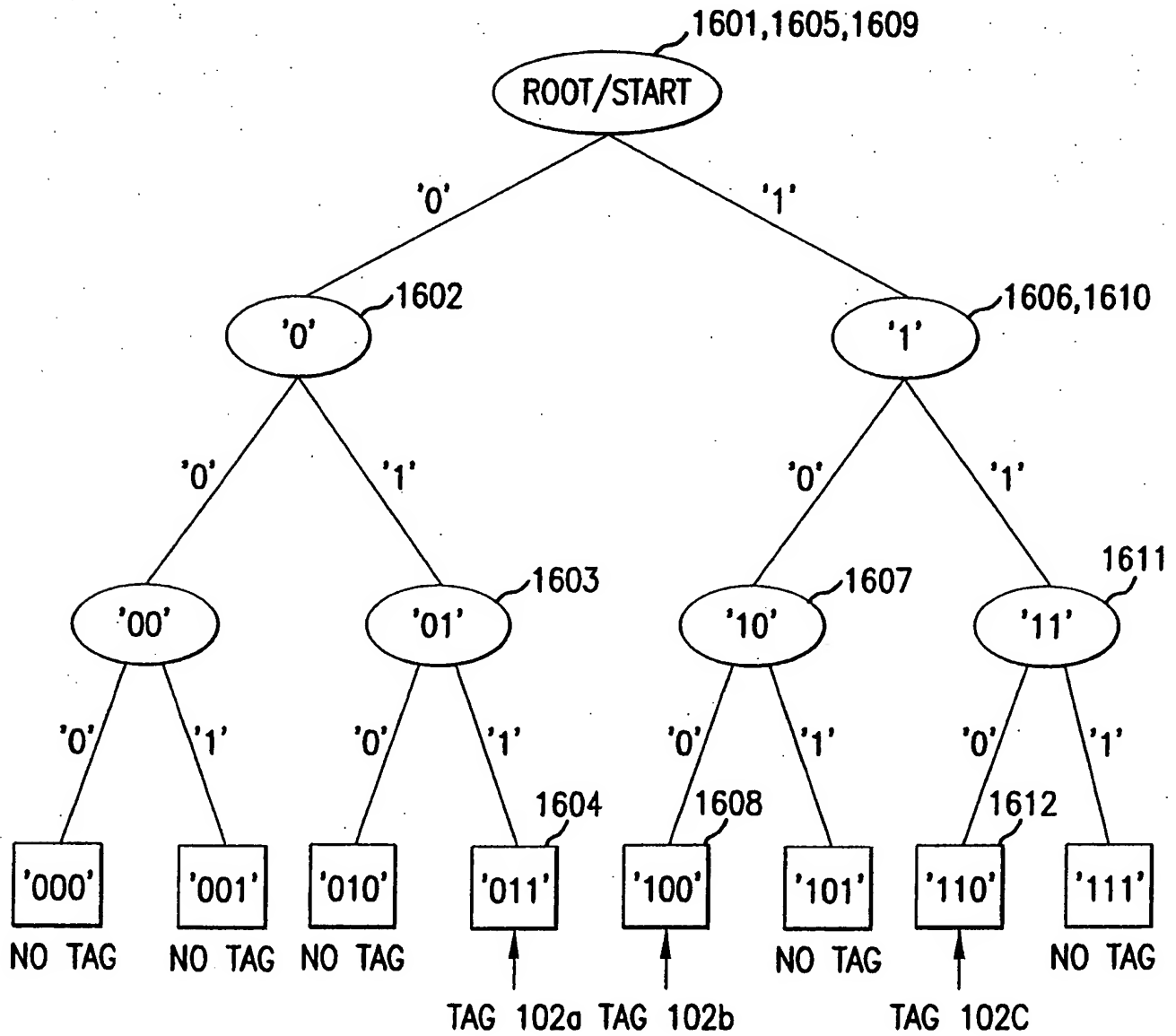


FIG. 16

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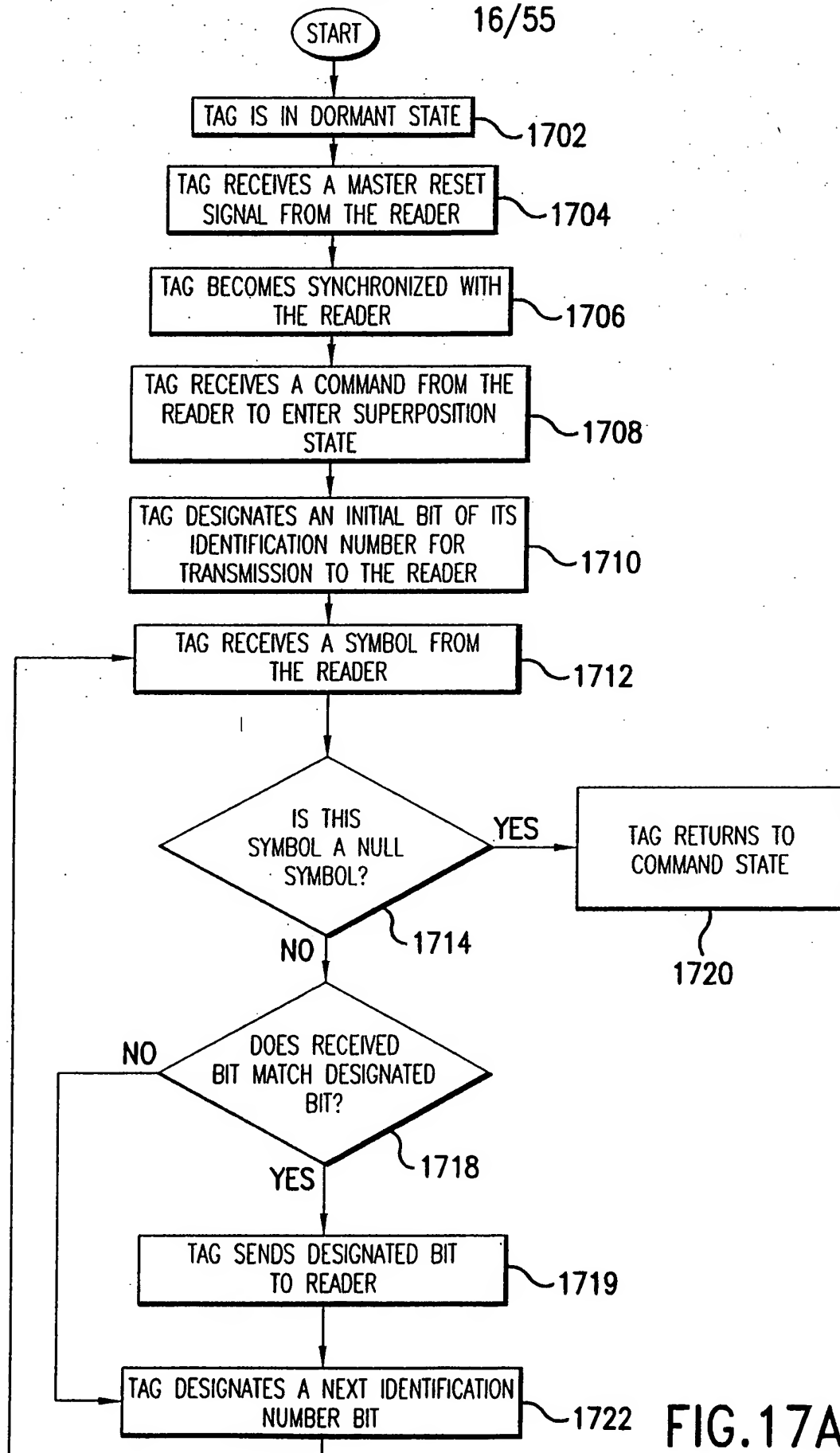


FIG. 17A

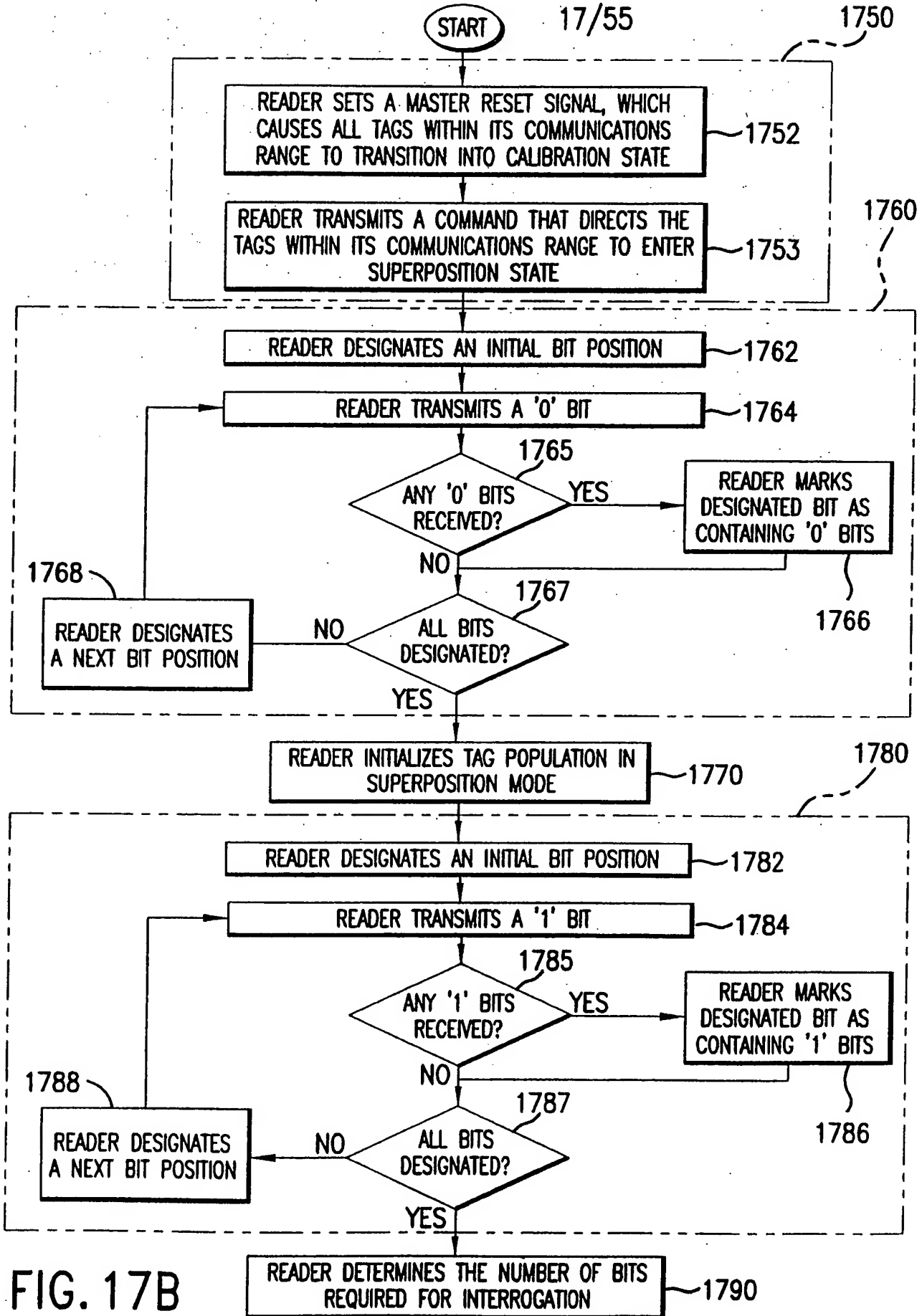


FIG. 17B

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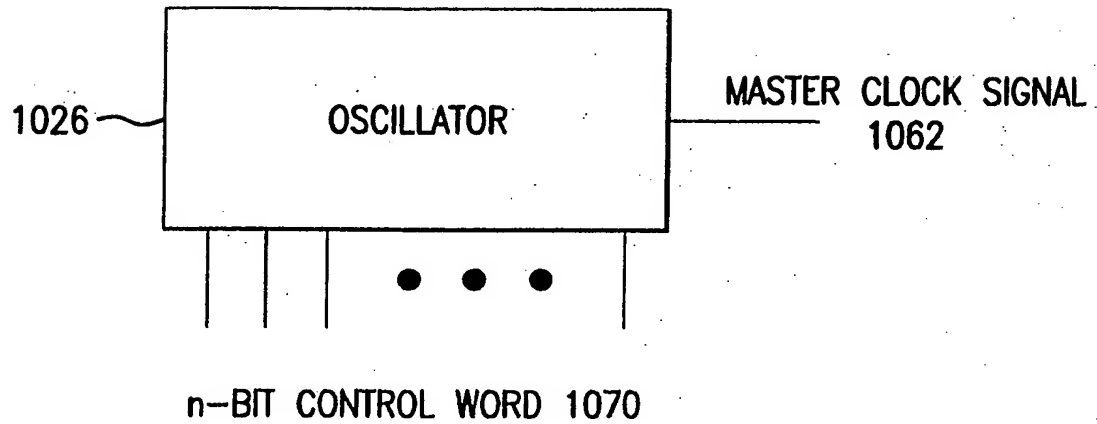


FIG. 18

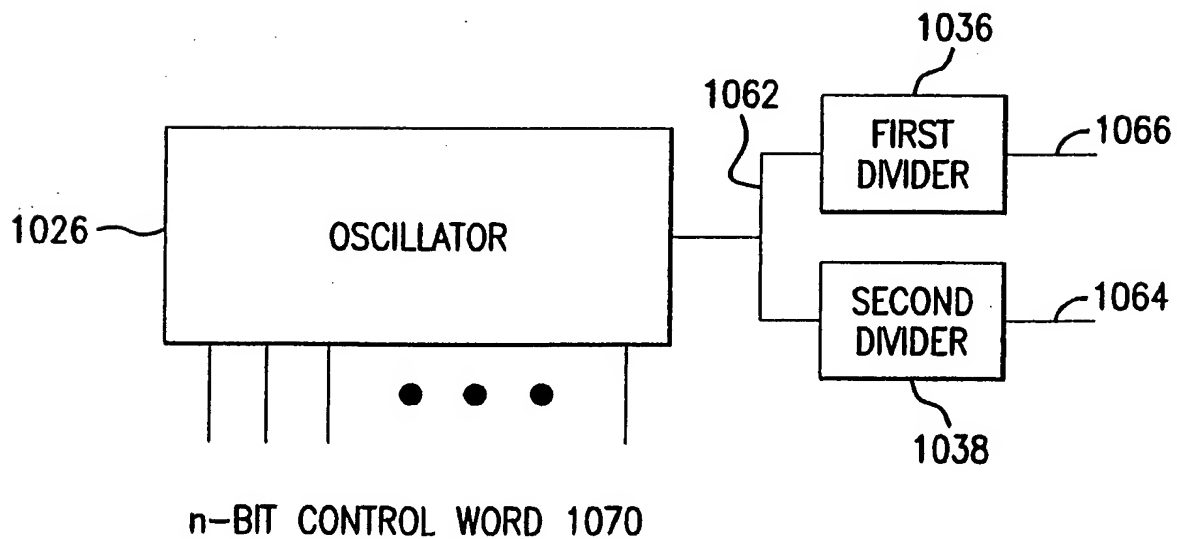


FIG. 19

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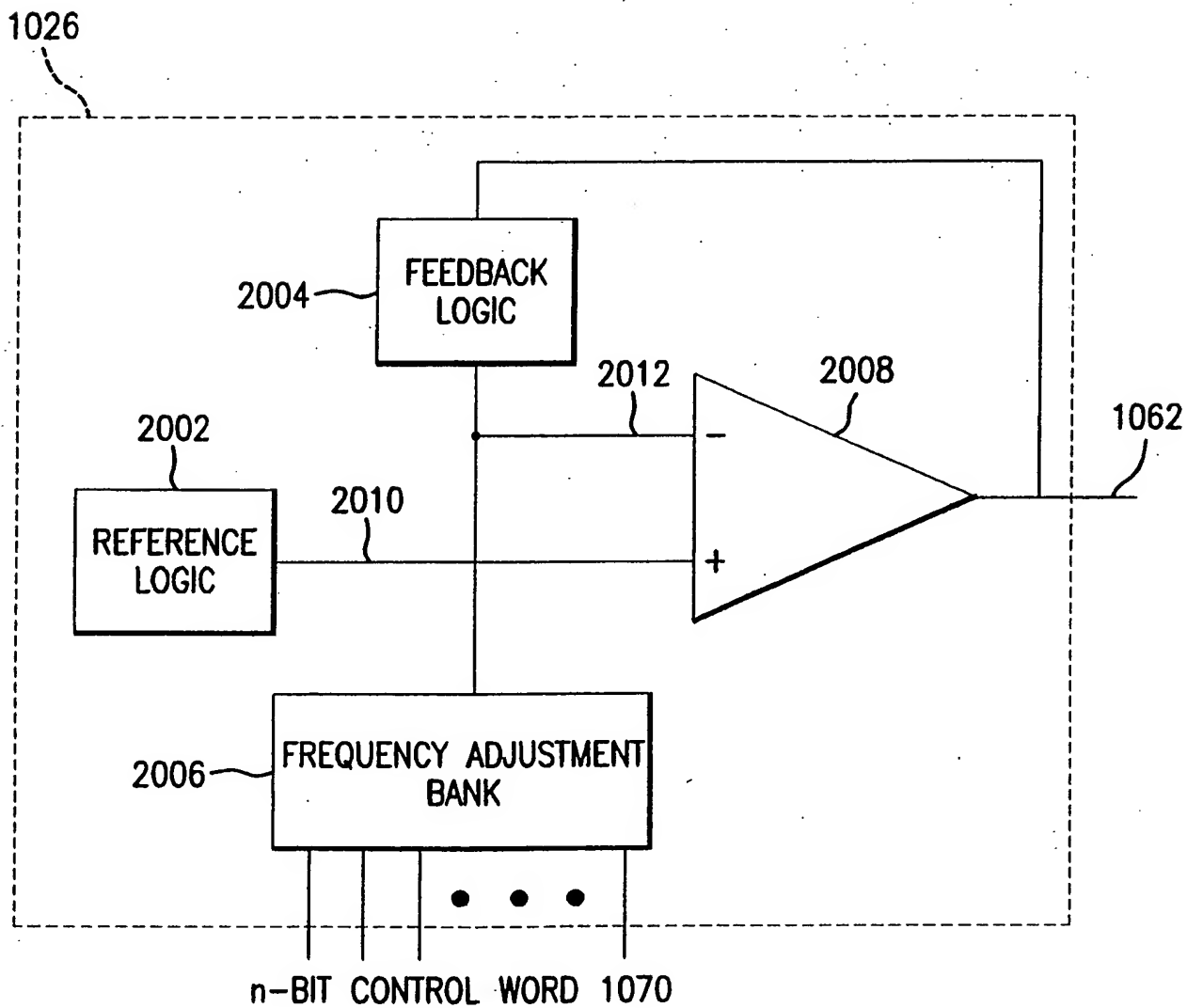


FIG. 20

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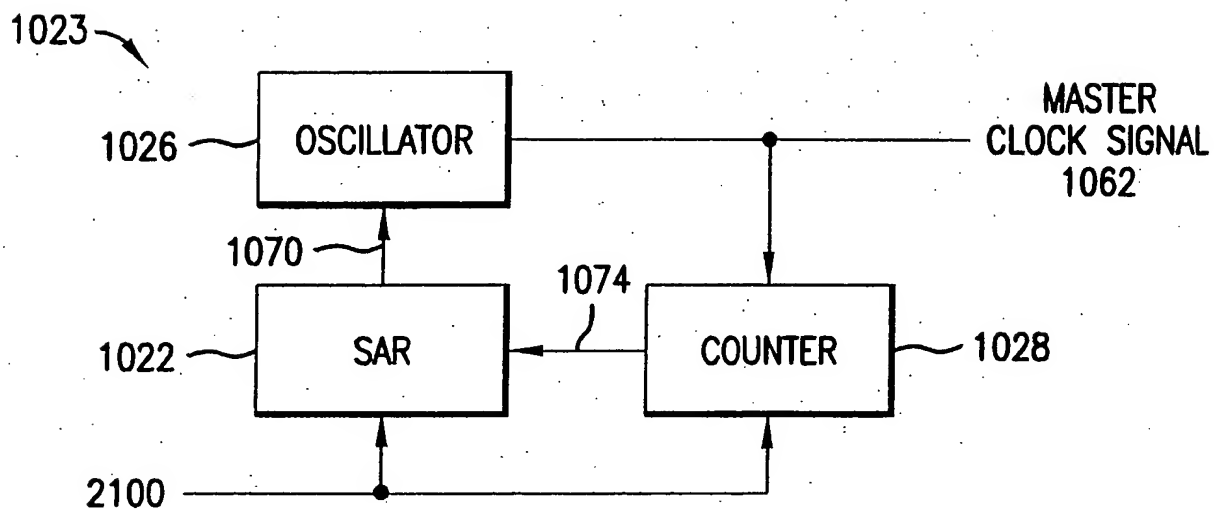


FIG. 21A

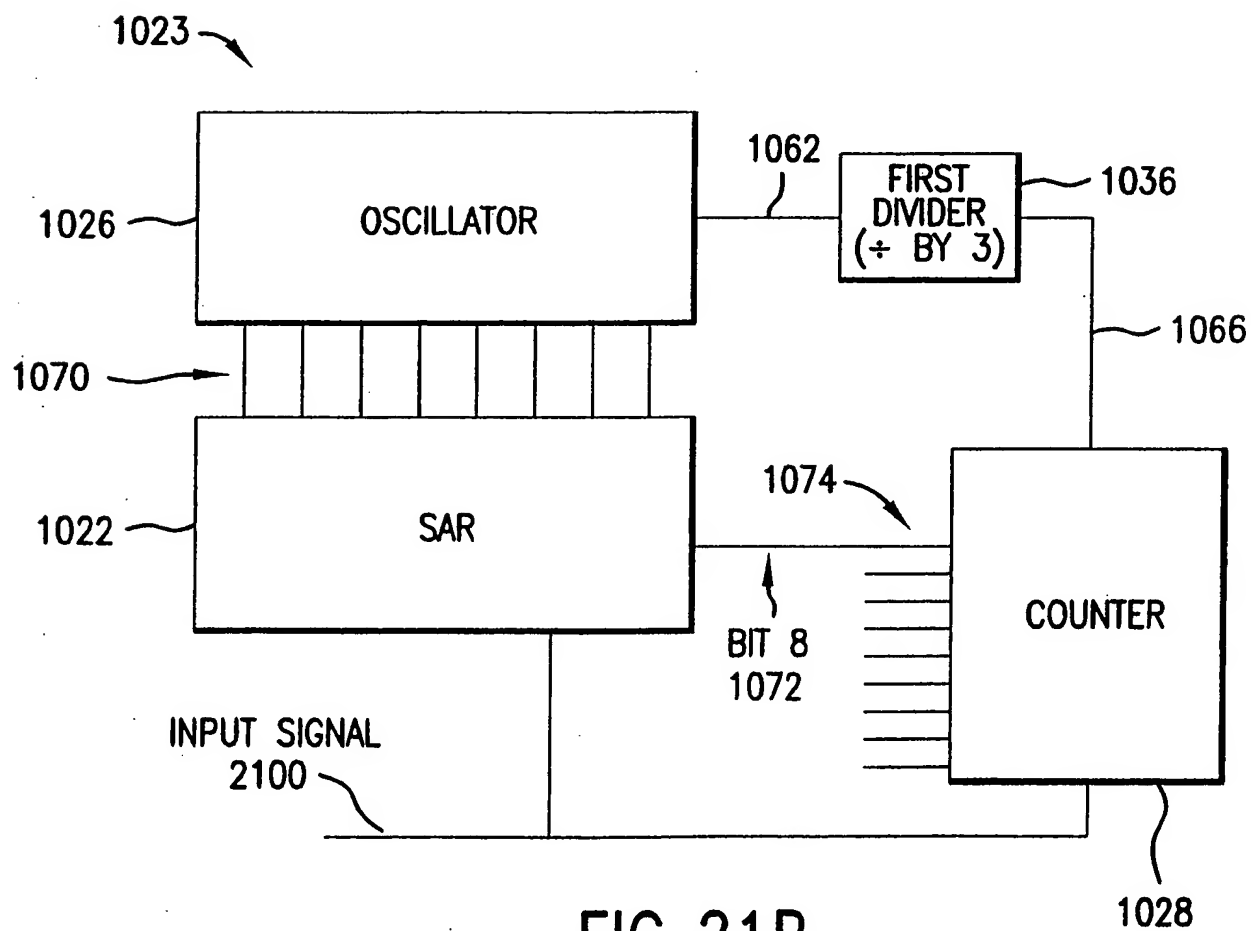
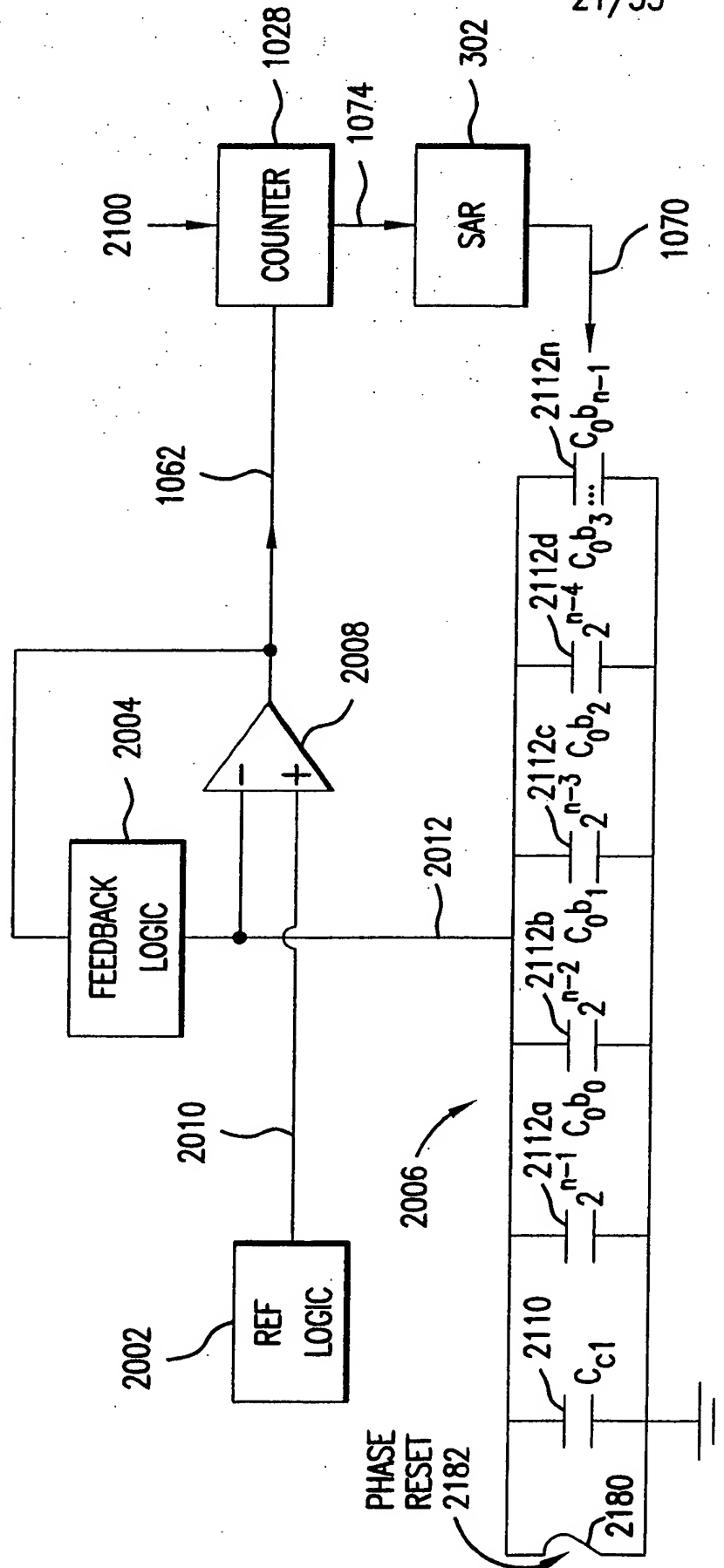


FIG. 21B

FIG. 21C



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PHYSICAL IMPLEMENTATION OF ADJUSTABLE CAPACITOR BANK

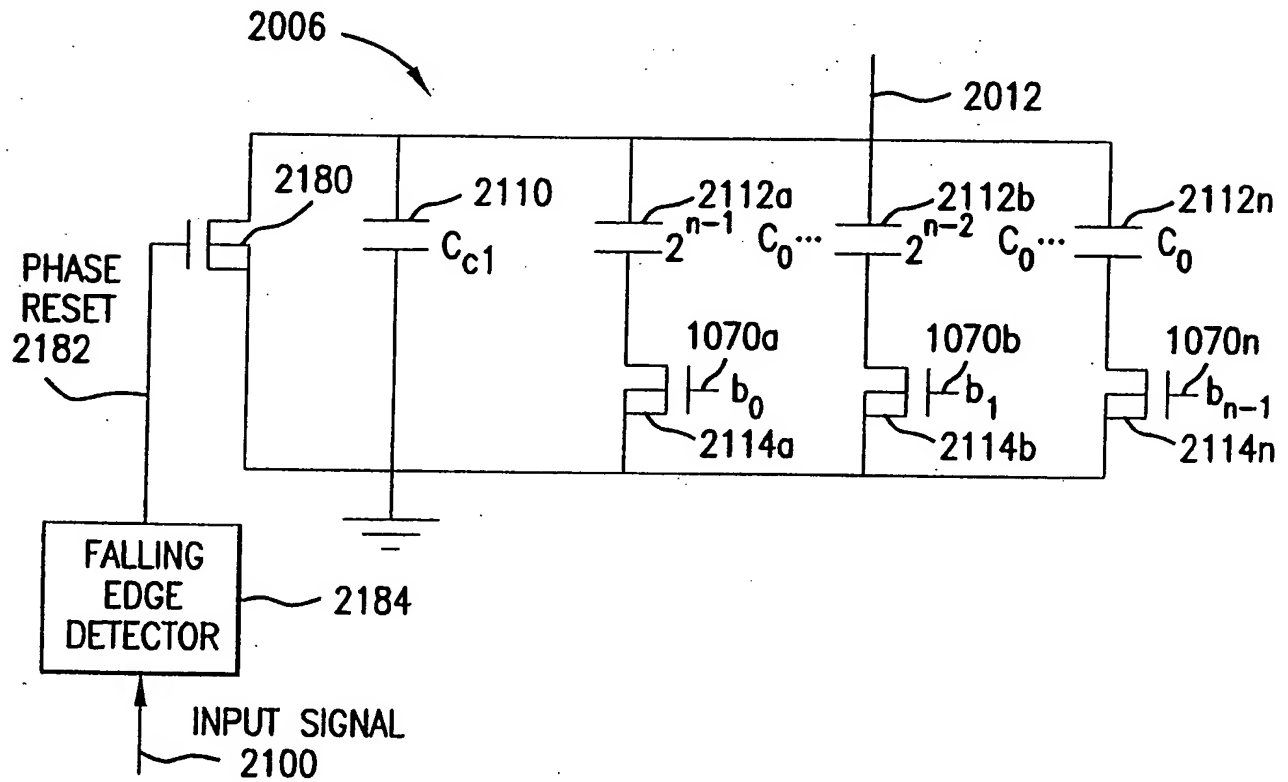
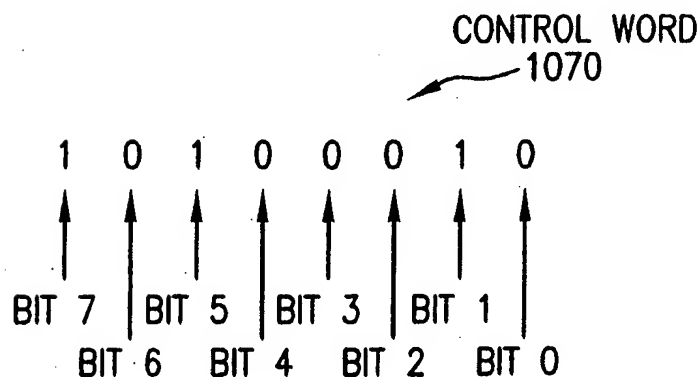
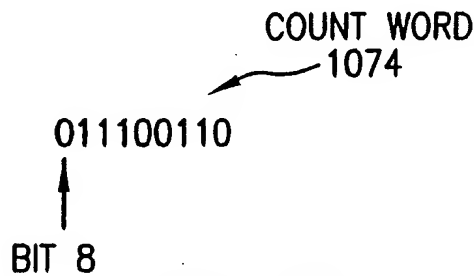
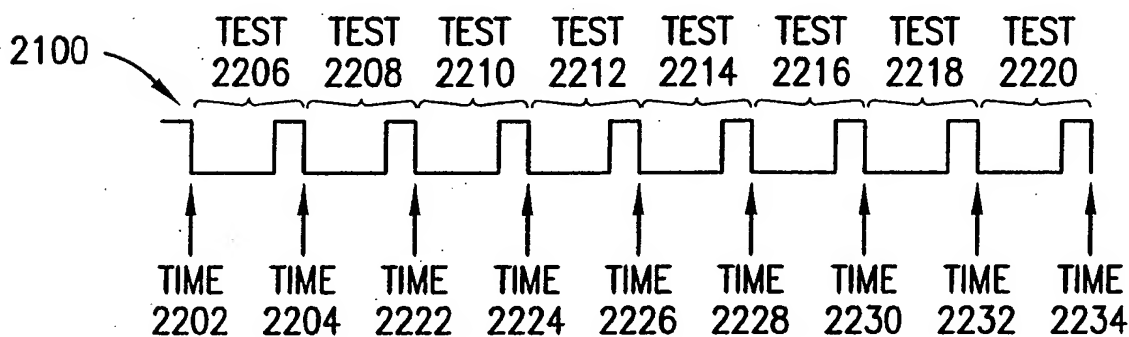
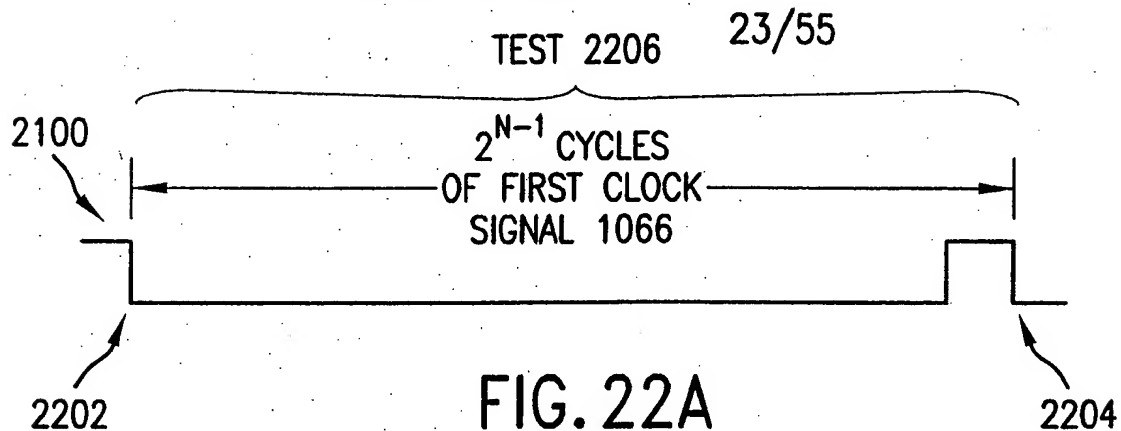


FIG. 21D



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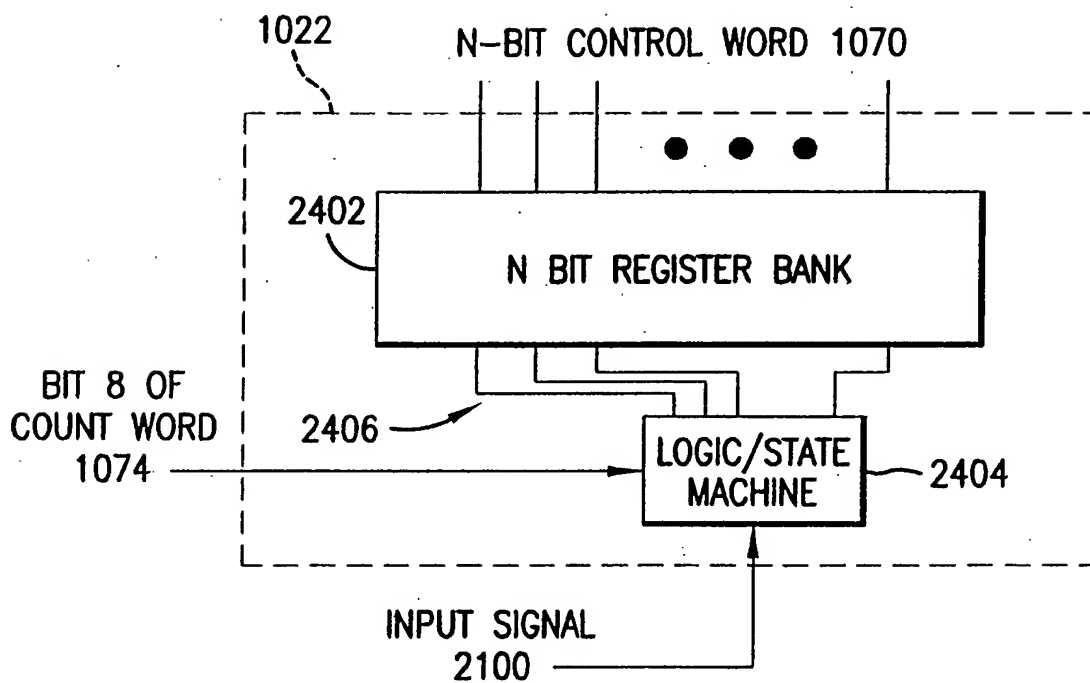


FIG. 24

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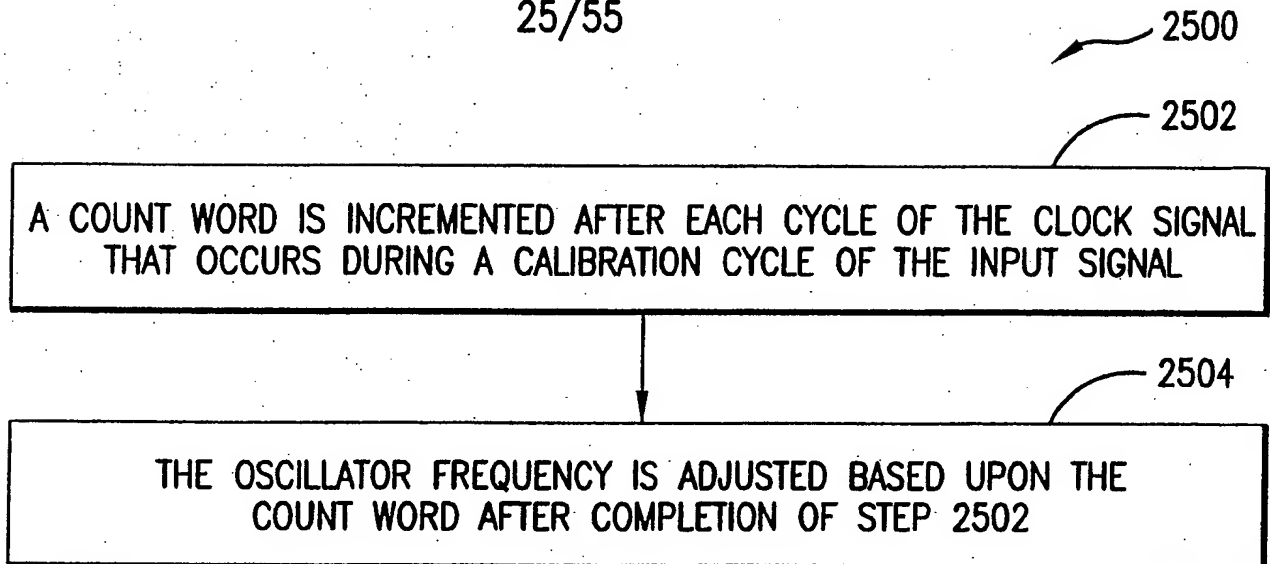


FIG. 25A

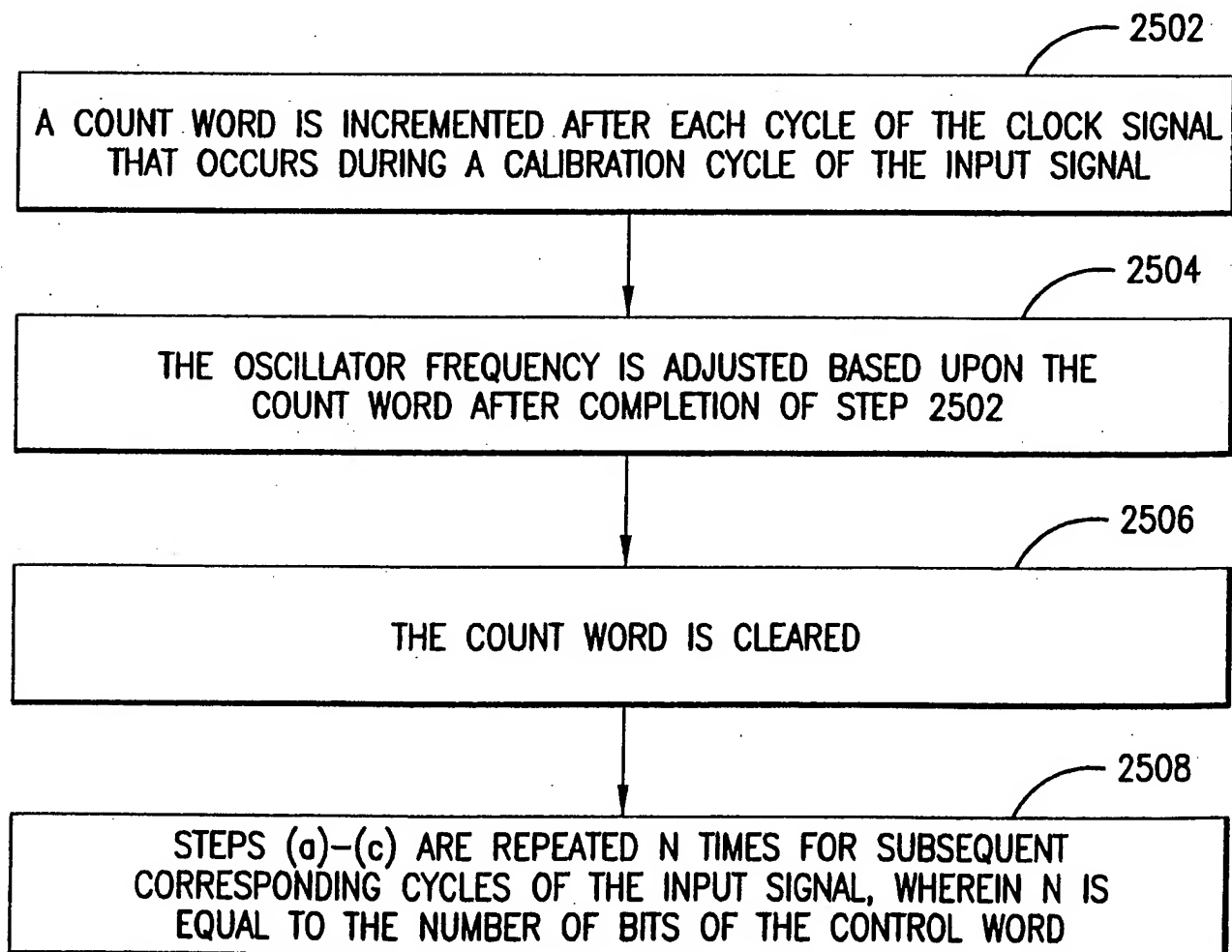


FIG. 25B

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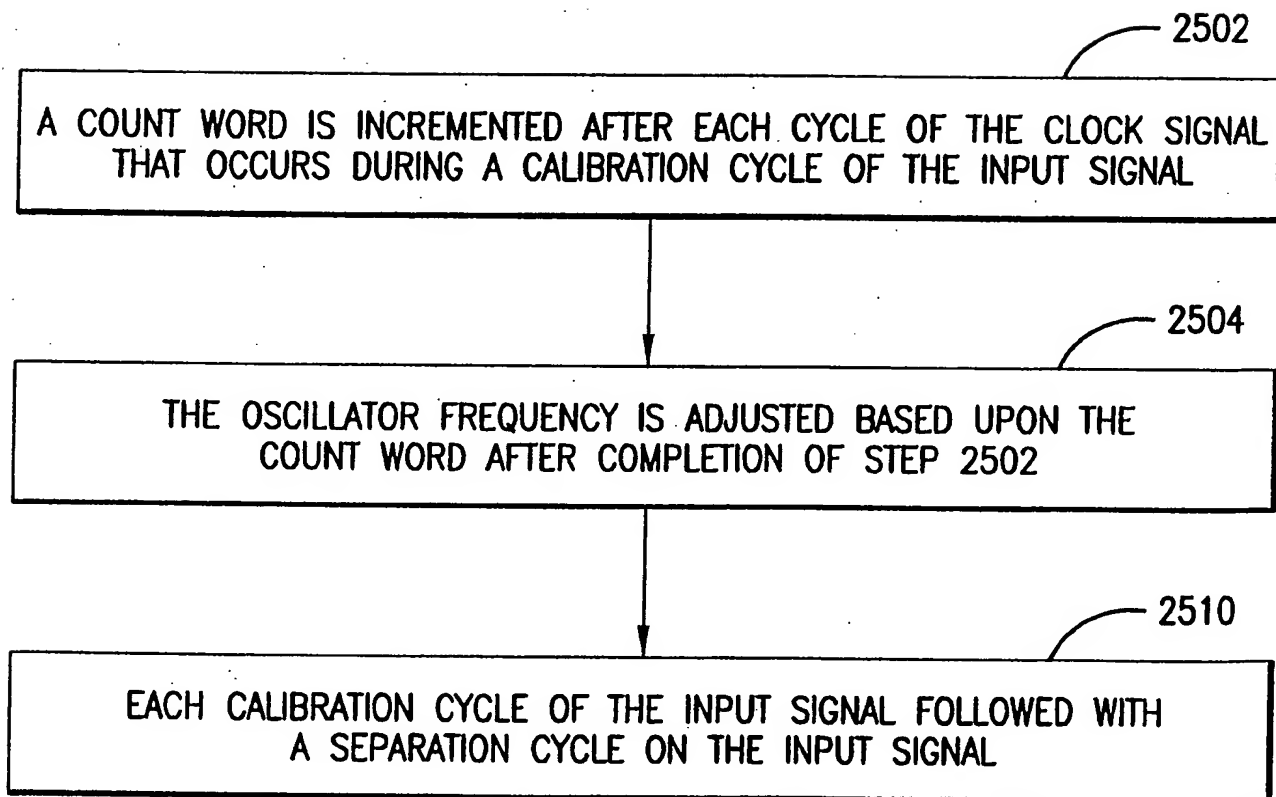


FIG. 25C

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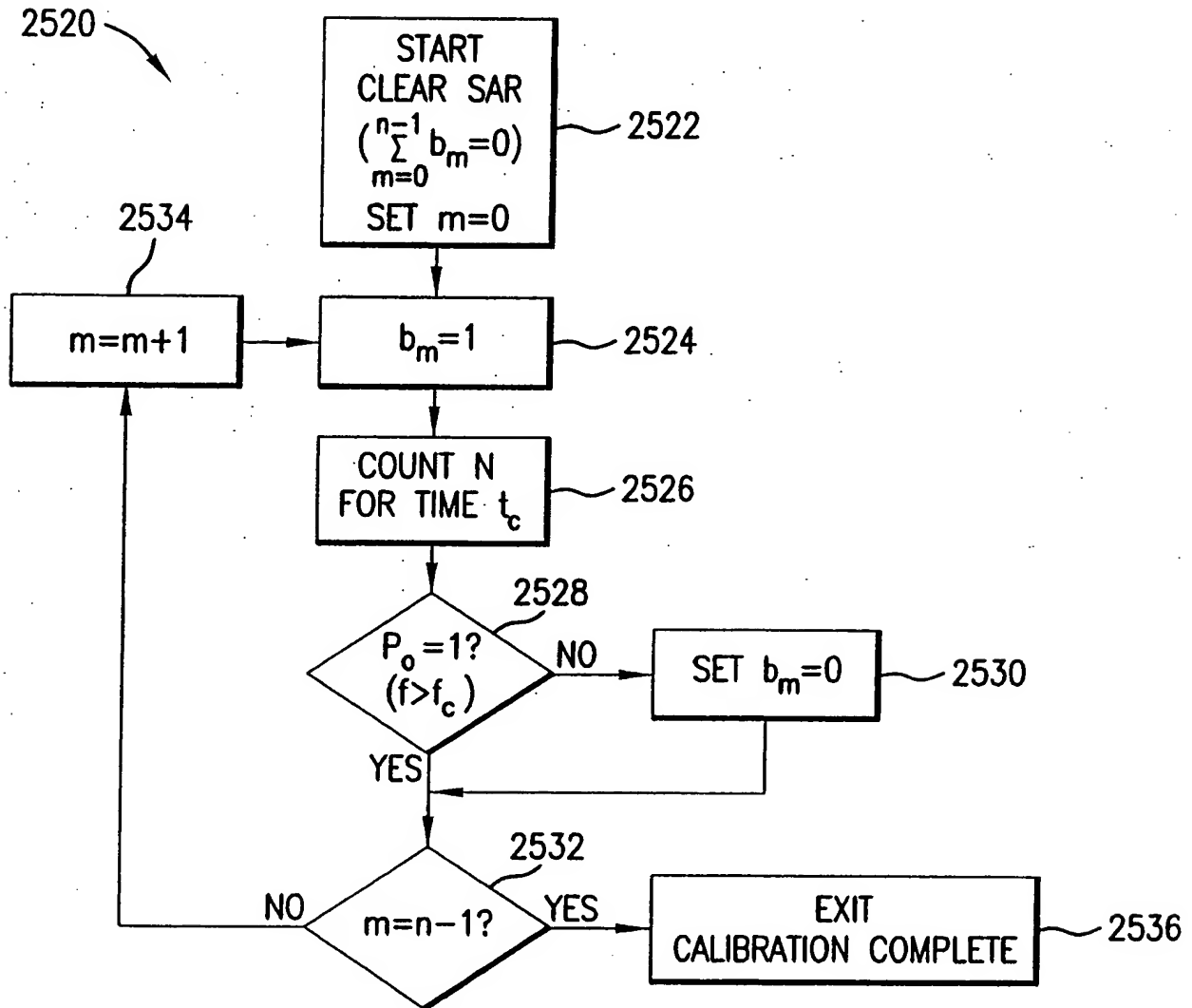


FIG. 25D

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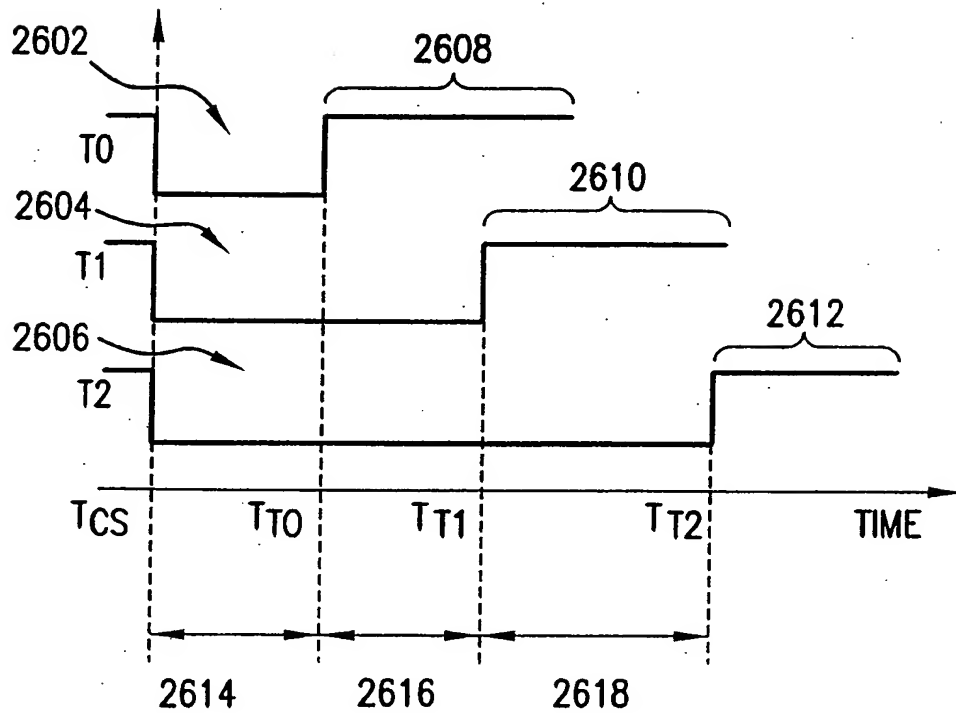


FIG.26A

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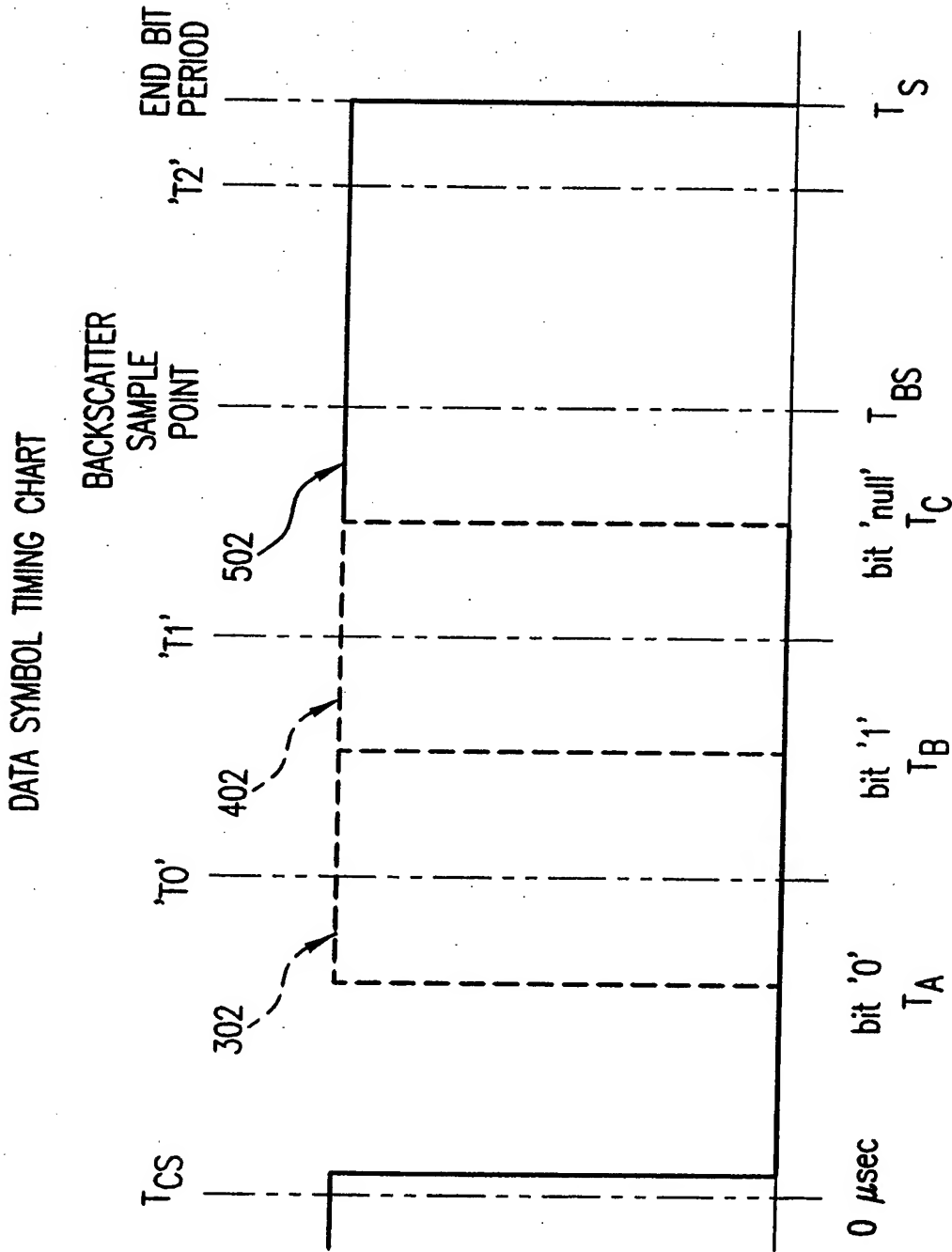


FIG.26B

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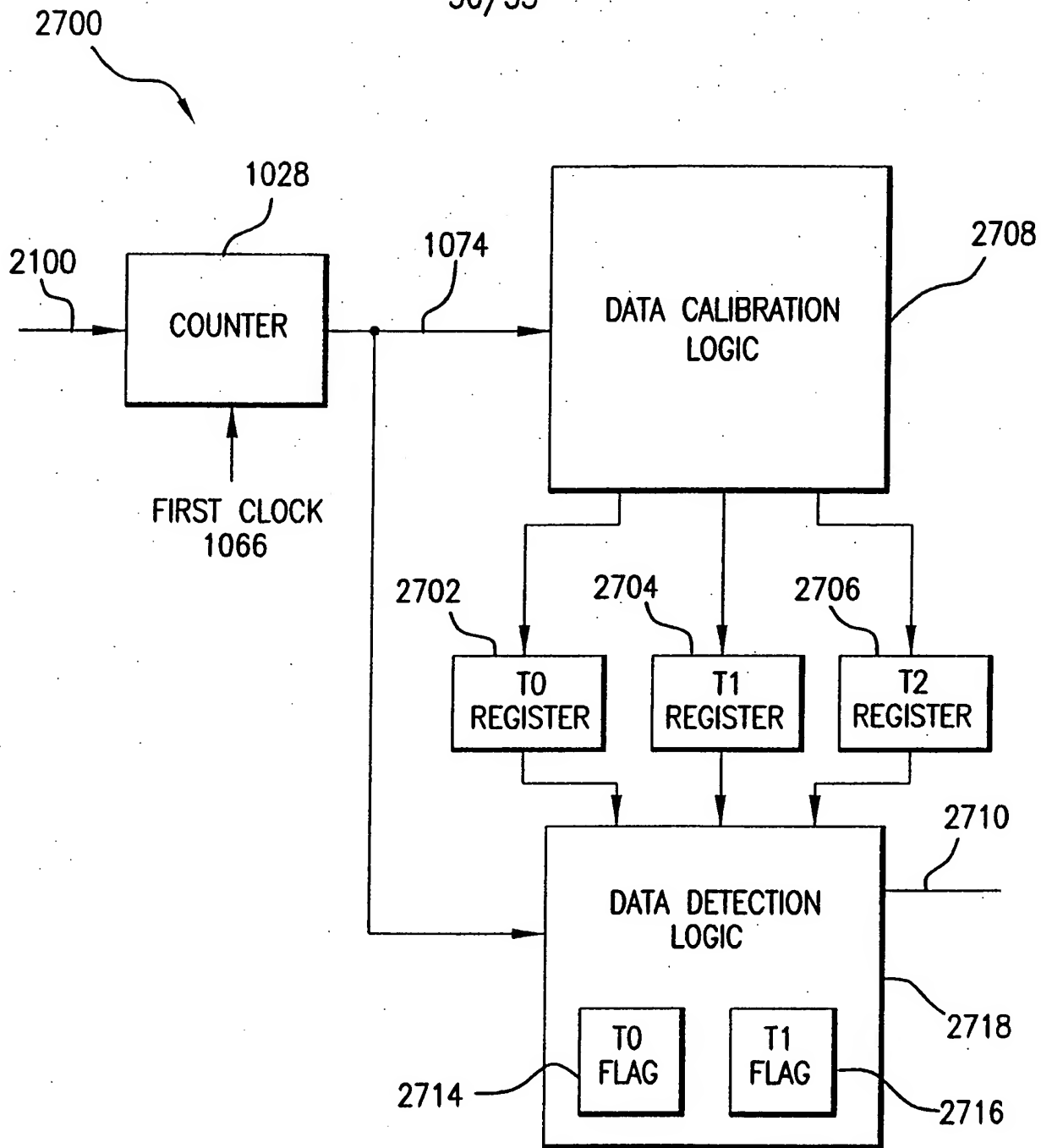


FIG.27

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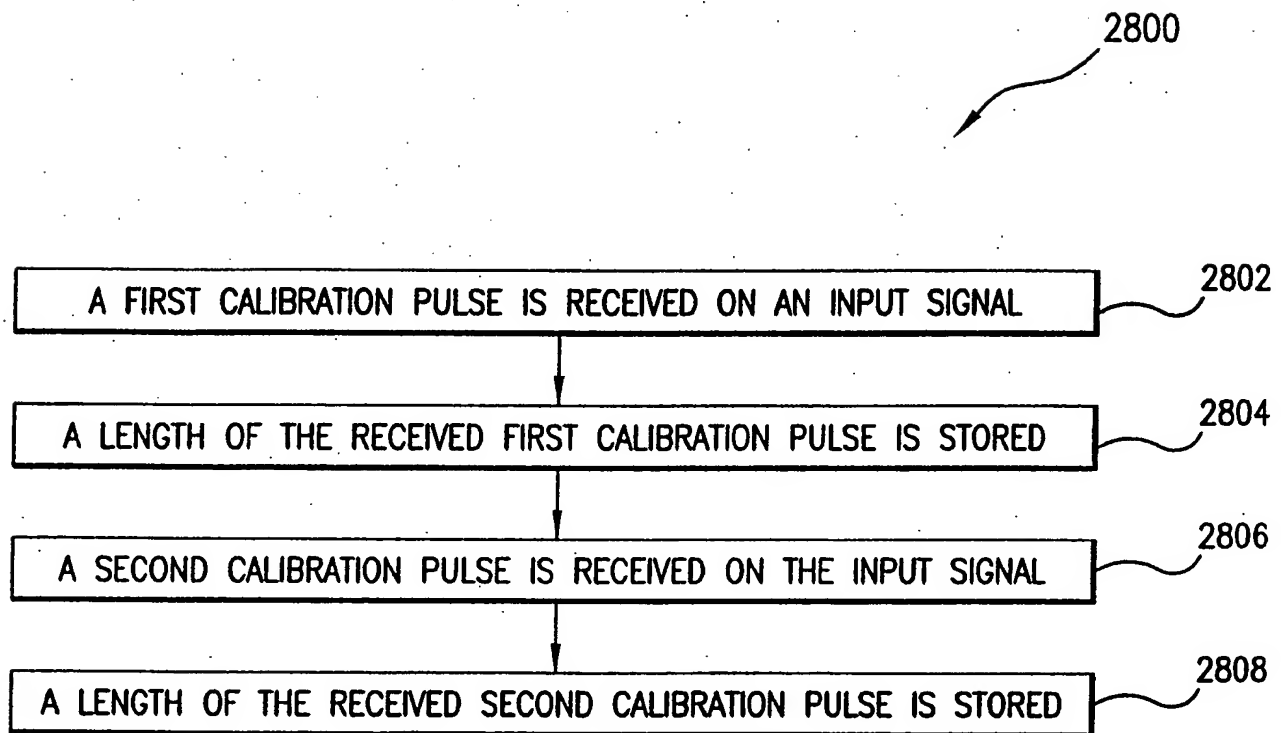


FIG.28A

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2800

FROM FLOWCHART 2800

2810

A DATA SYMBOL HAVING A PULSE PORTION IS RECEIVED ON THE INPUT SIGNAL, WHEREIN THE PULSE PORTION HAS A LENGTH

2812

A FIRST FLAG IS SET IF THE LENGTH OF THE PULSE PORTION IS GREATER THAN OR EQUAL TO THE STORED LENGTH OF THE FIRST CALIBRATION PULSE

2814

A SECOND FLAG IS SET IF THE LENGTH OF THE PULSE PORTION IS GREATER THAN OR EQUAL TO THE STORED LENGTH OF THE SECOND CALIBRATION PULSE

2816

THE DATA SYMBOL IS DETERMINED TO BE A FIRST LOGICAL VALUE IF THE FIRST FLAG IS NOT SET DURING STEP 2812

2818

THE DATA SYMBOL IS DETERMINED TO BE A SECOND LOGICAL VALUE IF THE FIRST FLAG IS SET AND THE SECOND FLAG IS NOT SET

2820

THE DATA SYMBOL IS DETERMINED TO BE A THIRD LOGICAL VALUE IF THE FIRST FLAG IS SET AND THE SECOND FLAG IS SET

2822

THE FIRST LOGICAL VALUE IS DEFINED AS A LOGICAL 1 BIT

2824

THE SECOND LOGICAL VALUE IS DEFINED AS A LOGICAL 0 BIT

2826

THE THIRD LOGICAL VALUE IS DEFINED AS A LOGICAL NULL BIT

FIG.28B

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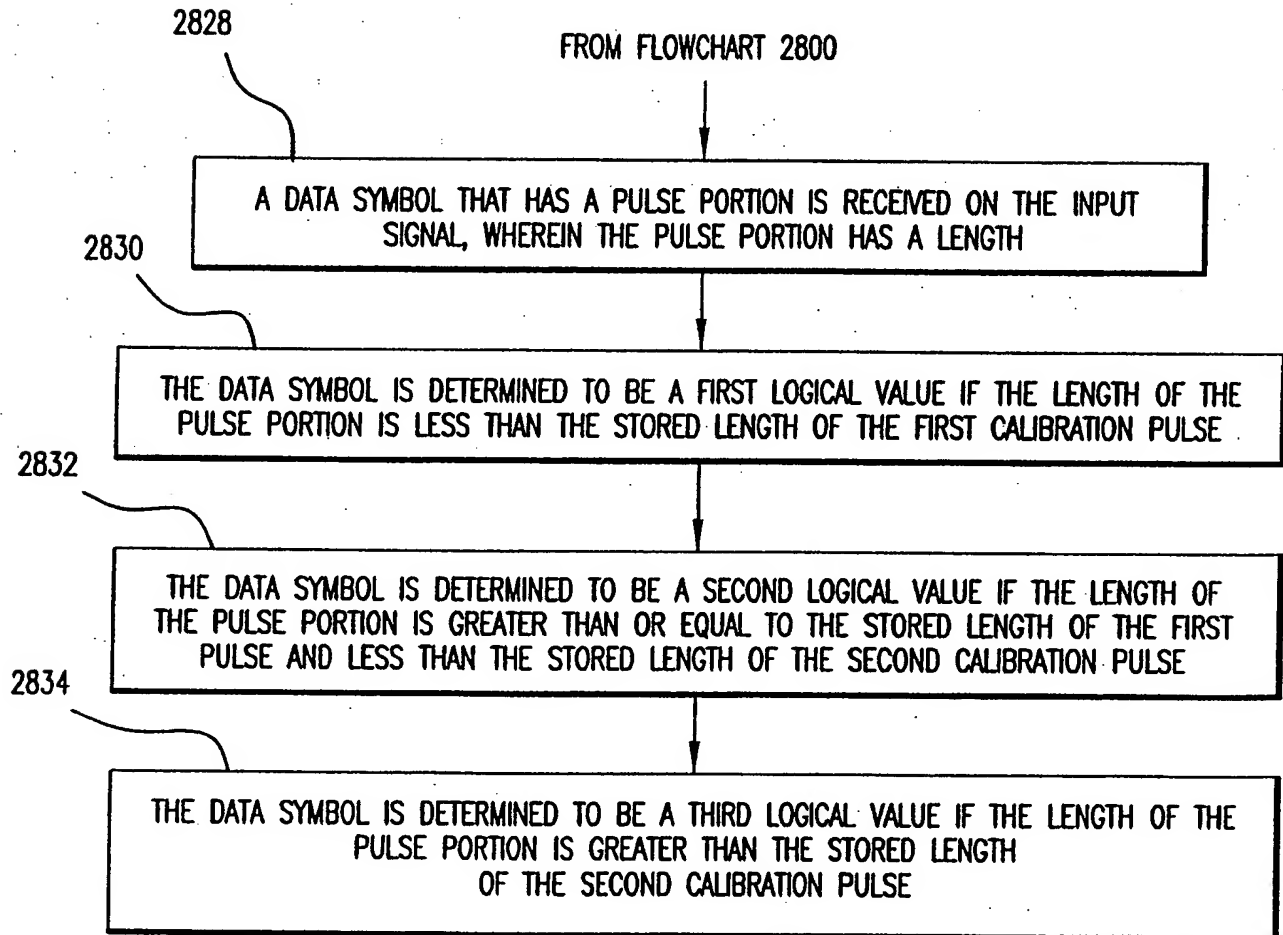


FIG.28C

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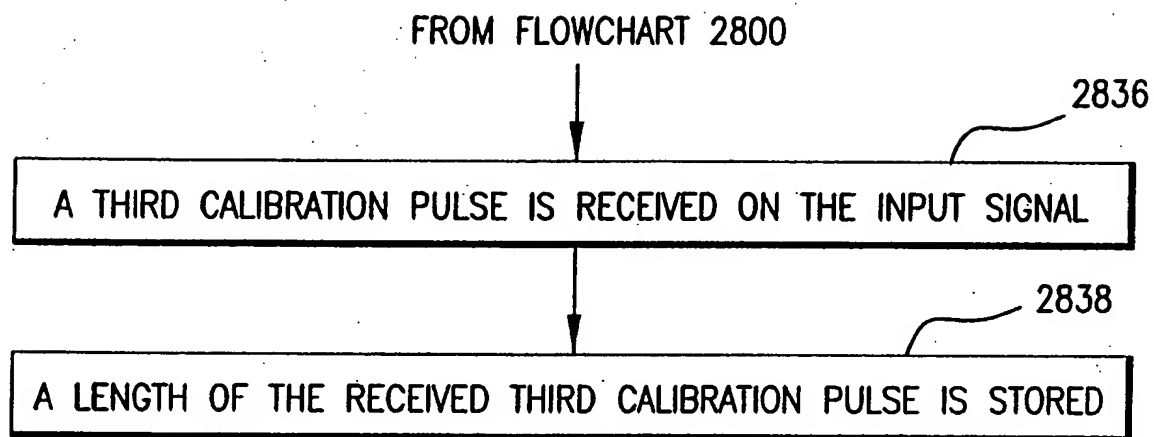
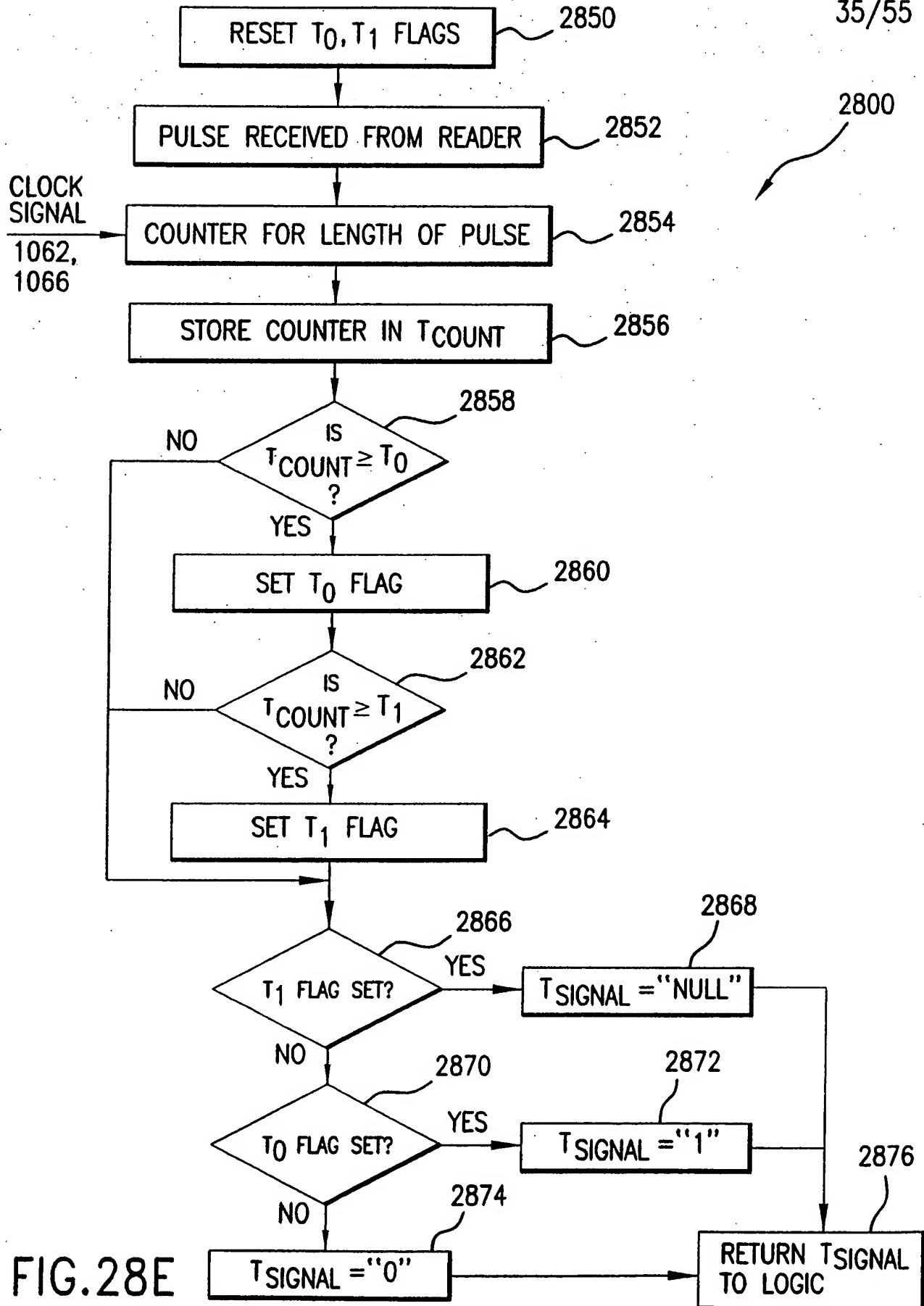


FIG.28D

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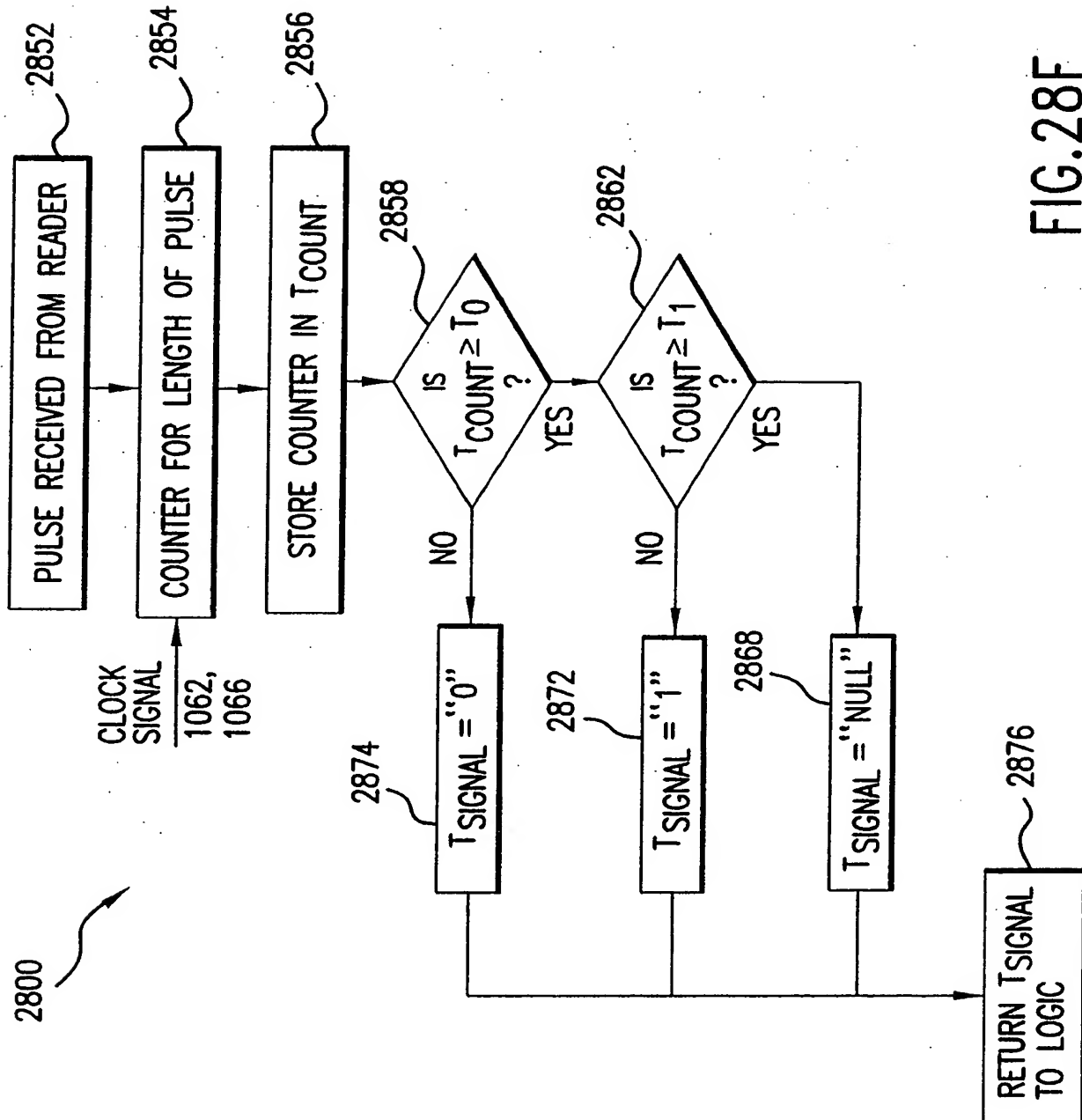


FIG. 28F

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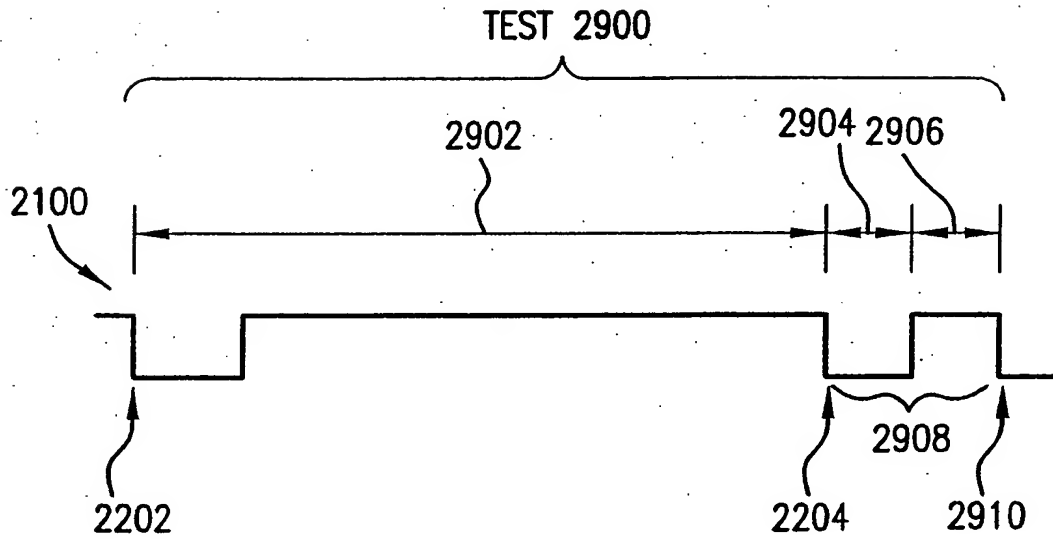


FIG.29



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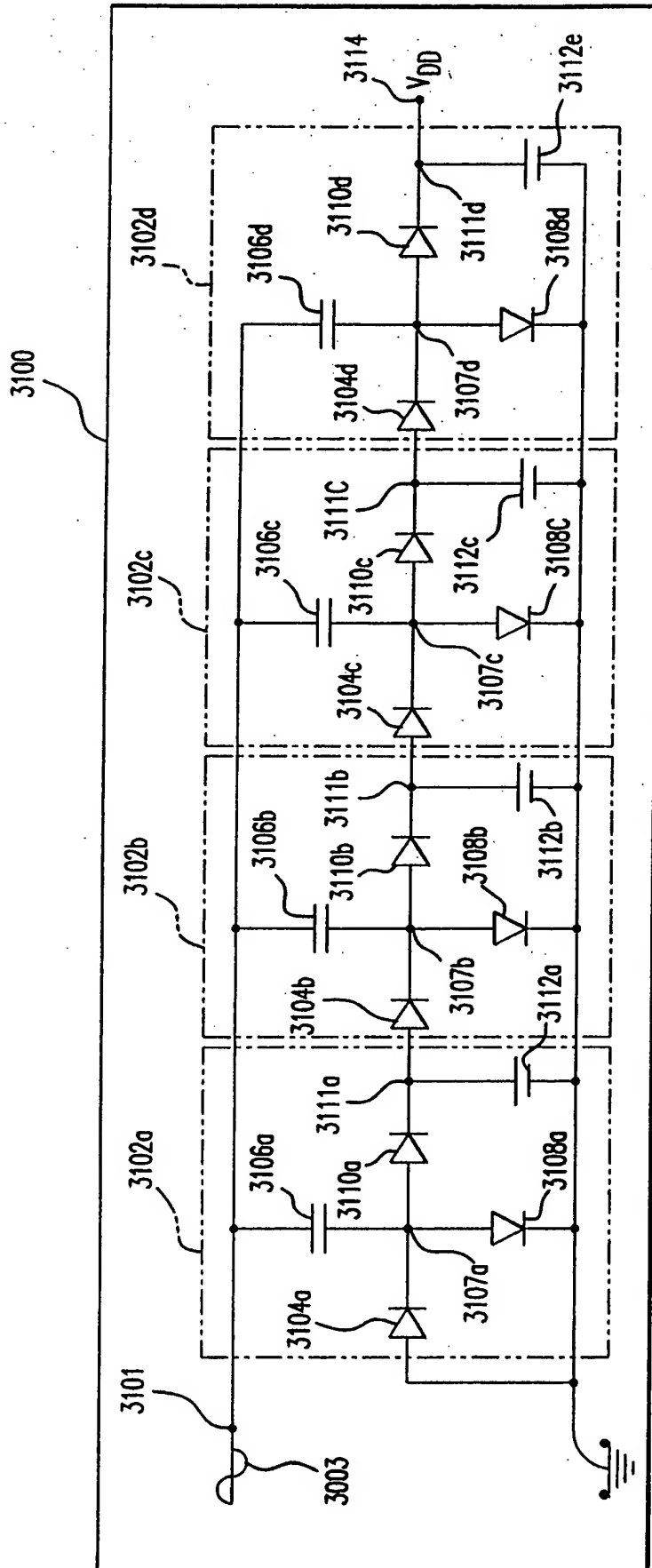


FIG.31

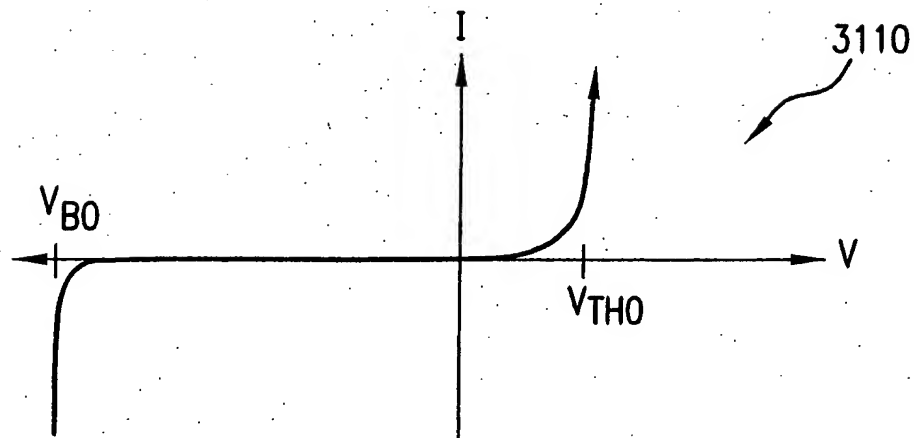


FIG. 32A

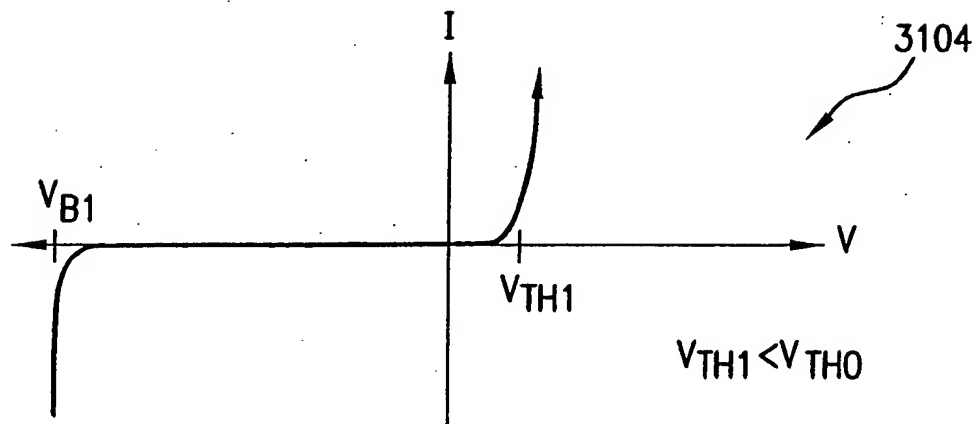


FIG. 32B

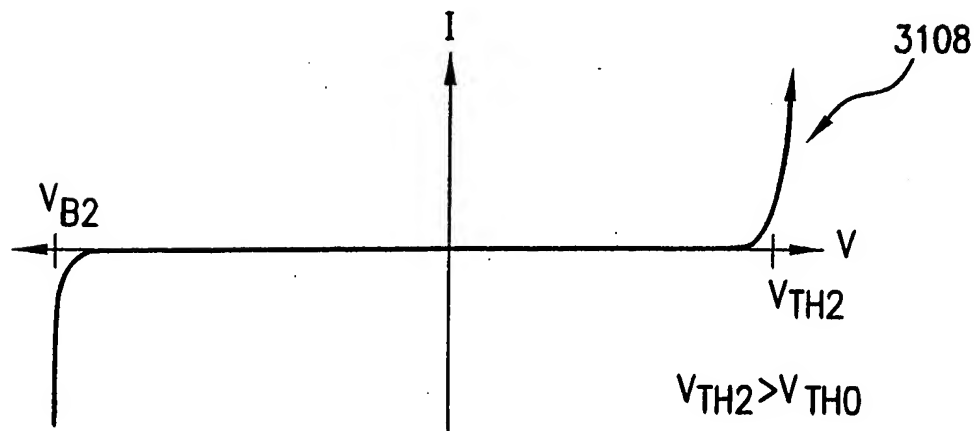


FIG. 32C

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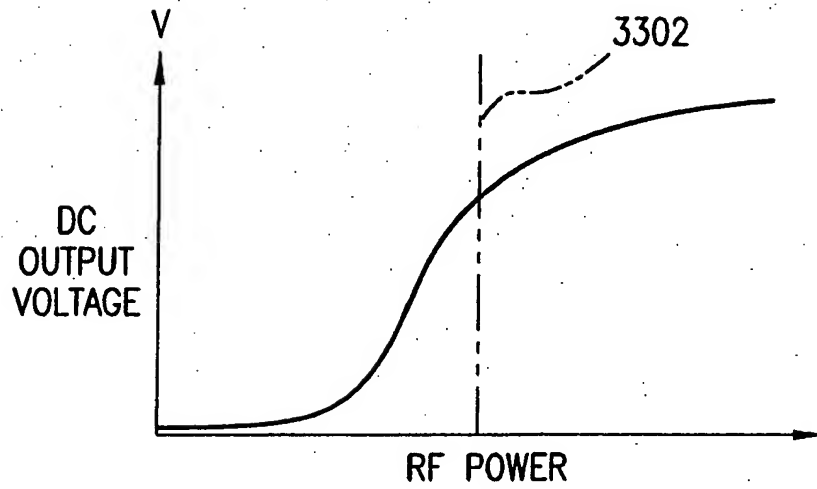


FIG.33A

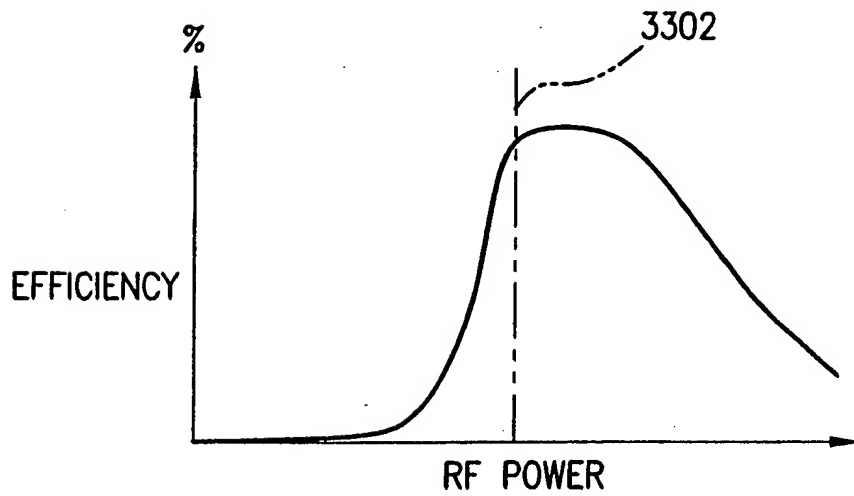


FIG.33B

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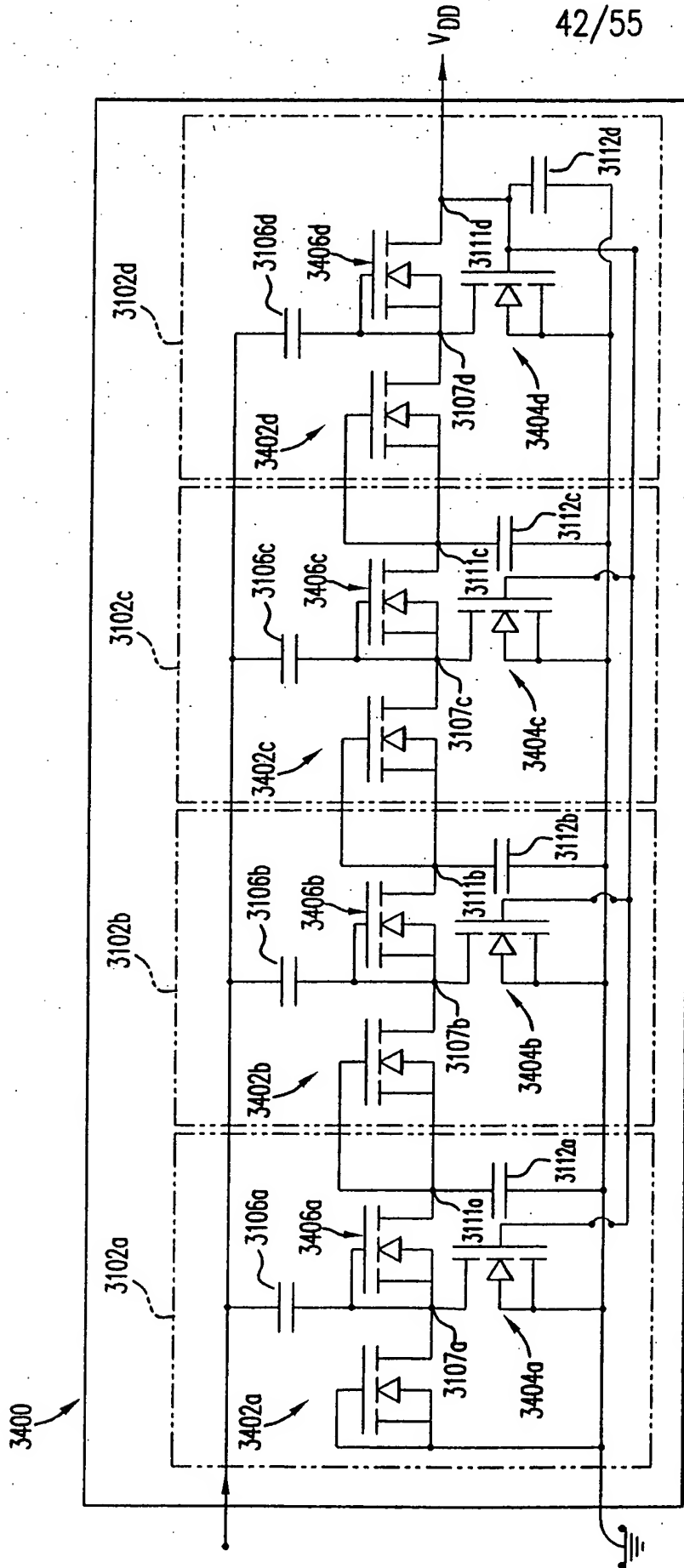


FIG. 34A

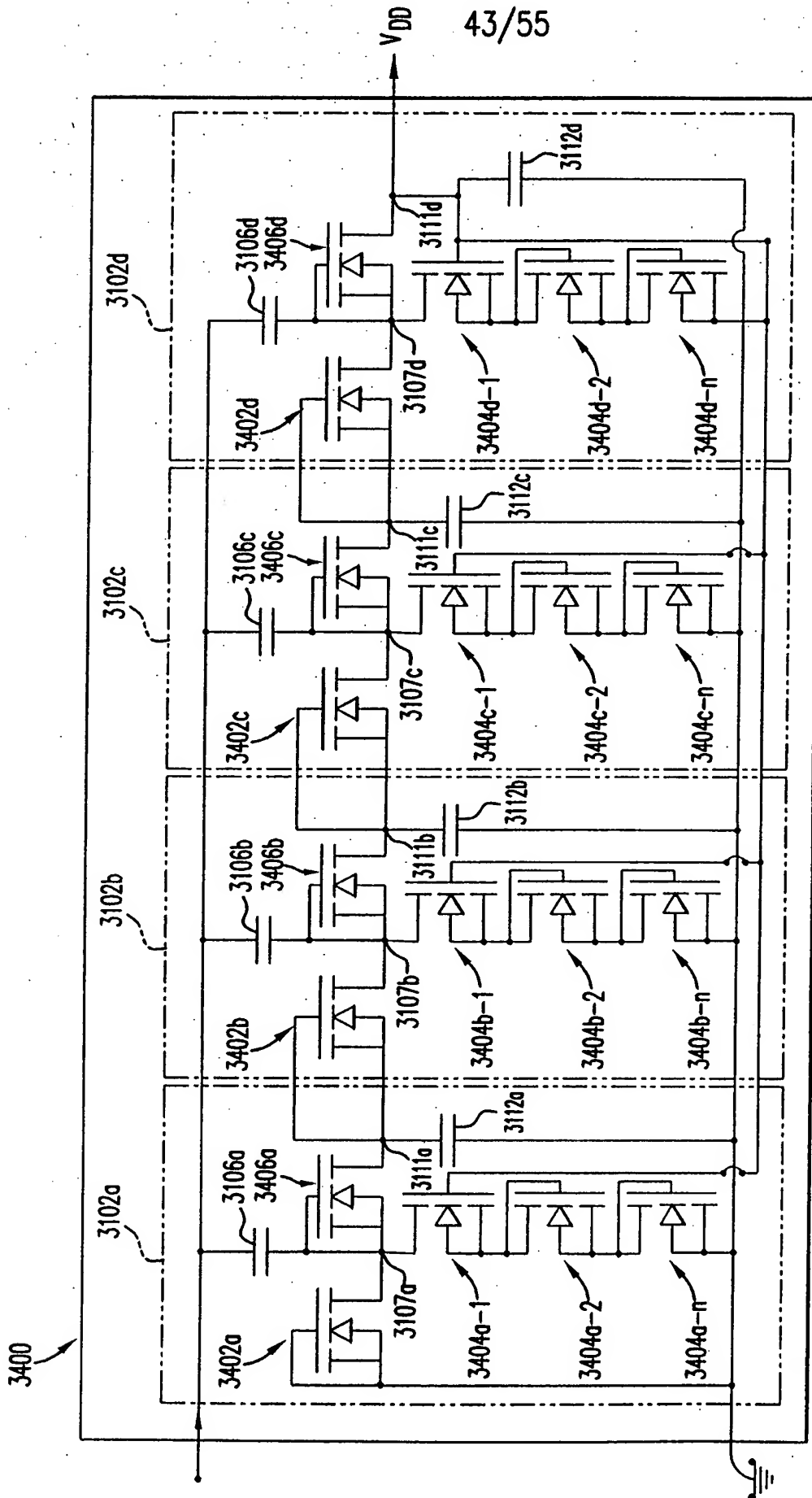


FIG. 34B

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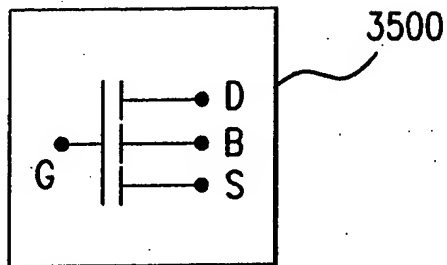
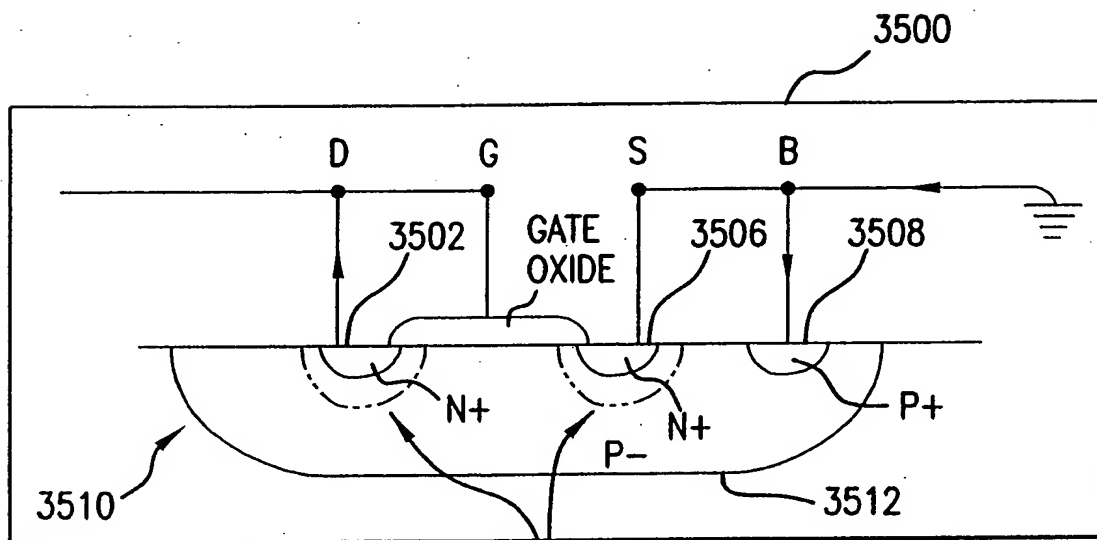


FIG.35A



ZERO BIASED
 DEPLETION
 REGION

FIG.35B

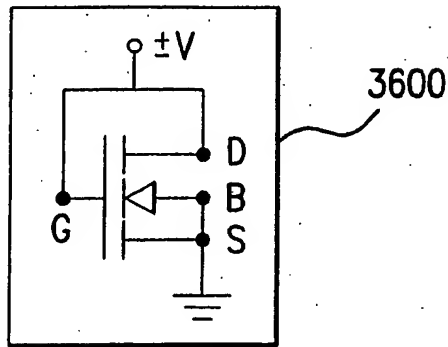


FIG.36A

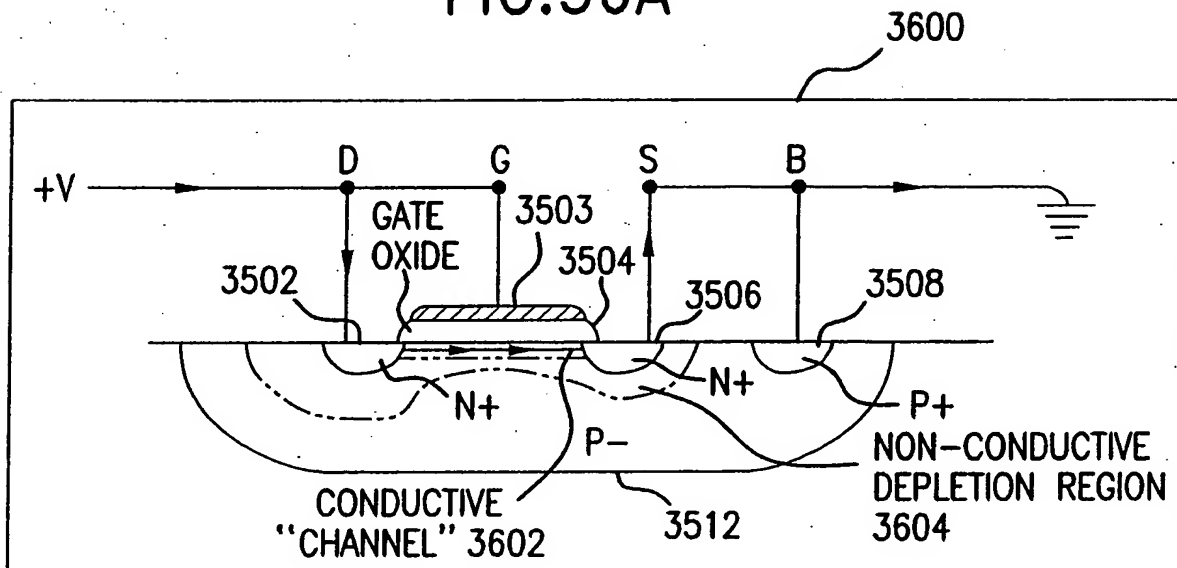


FIG.36B

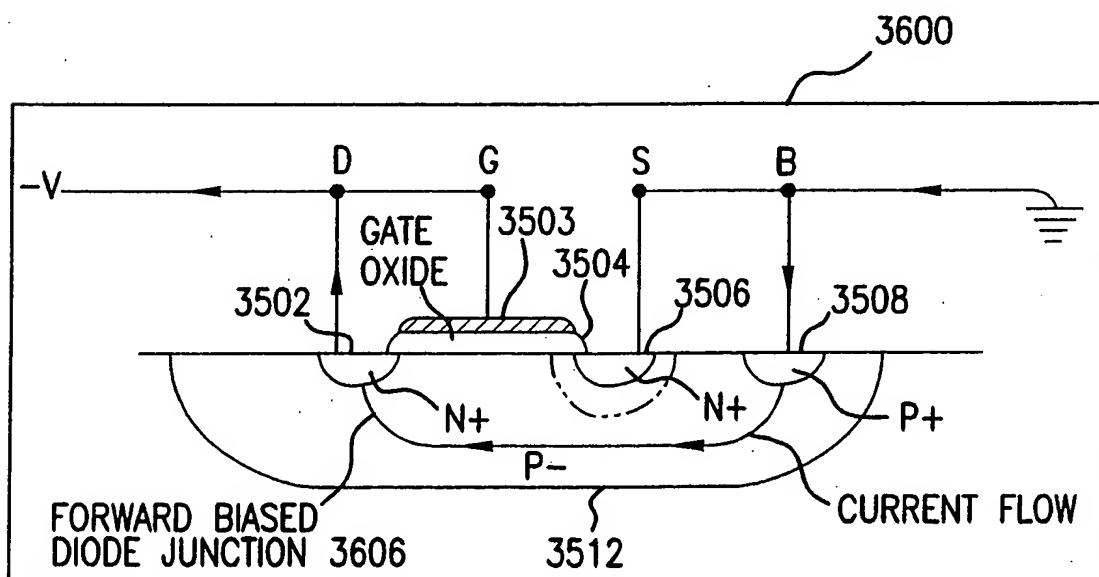


FIG.36C

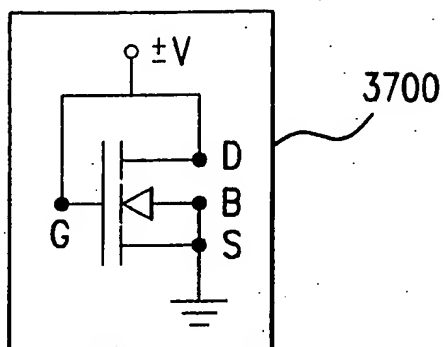


FIG.37A

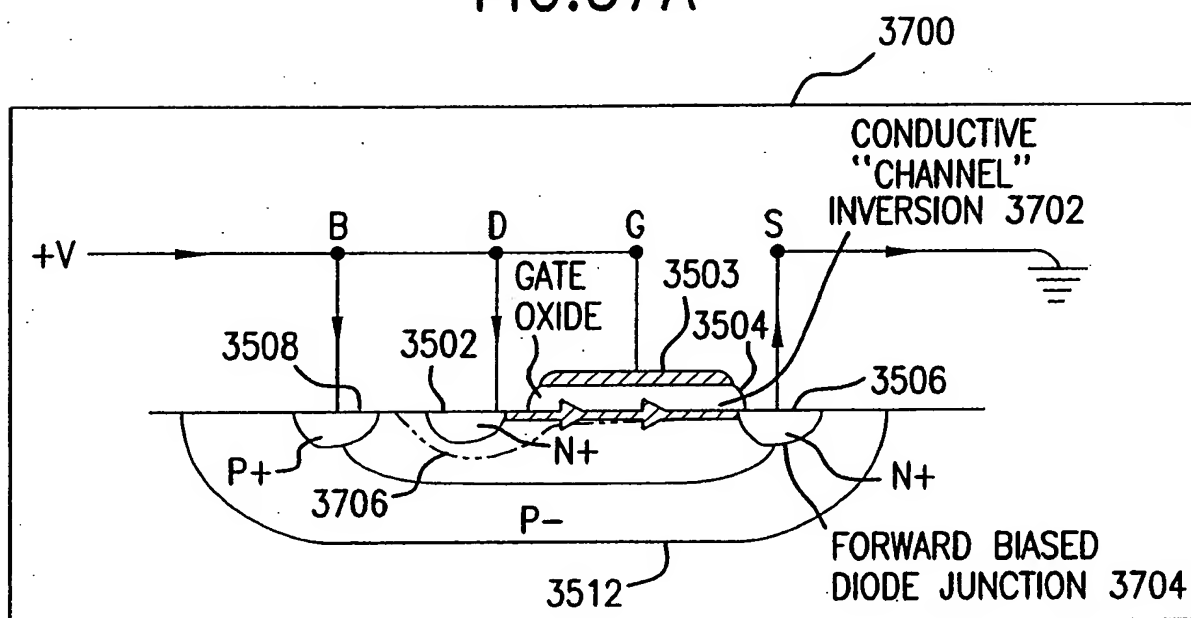


FIG.37B

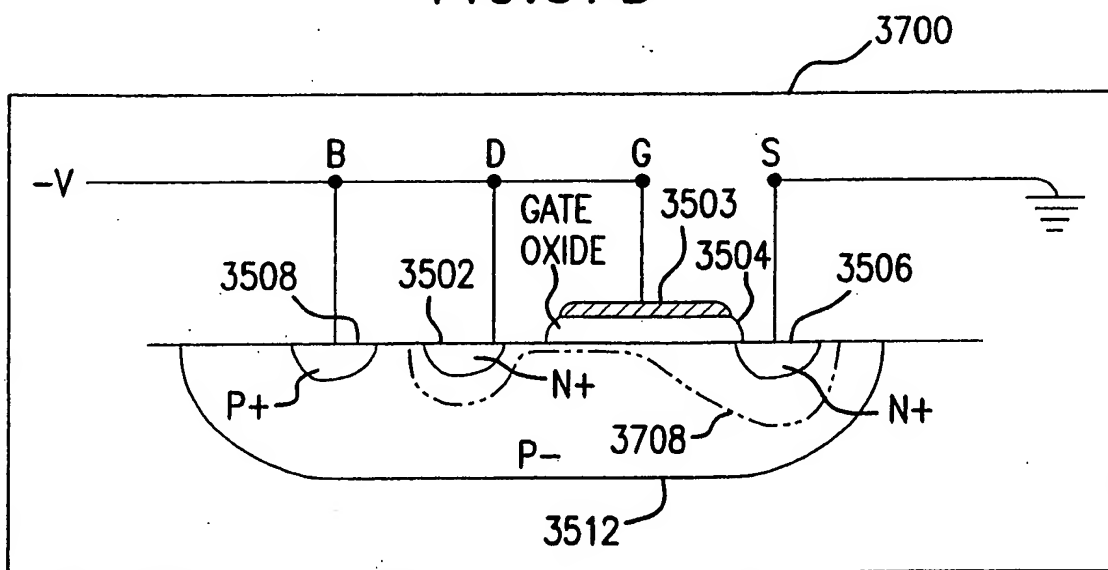


FIG.37C

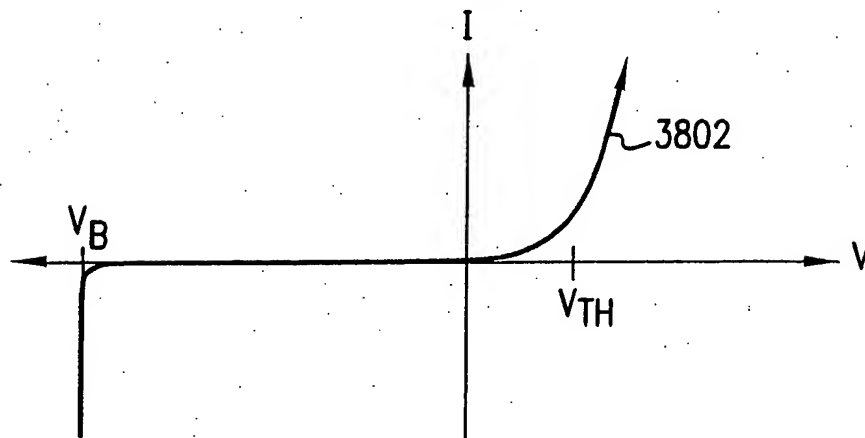


FIG. 38A

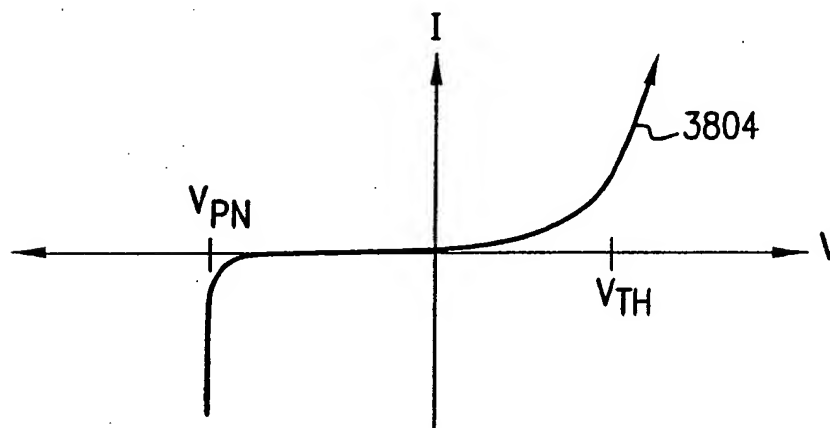


FIG. 38B

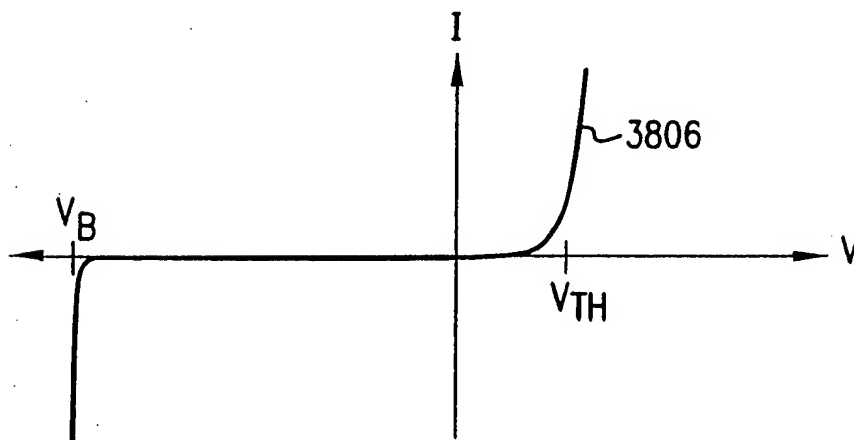


FIG. 38C

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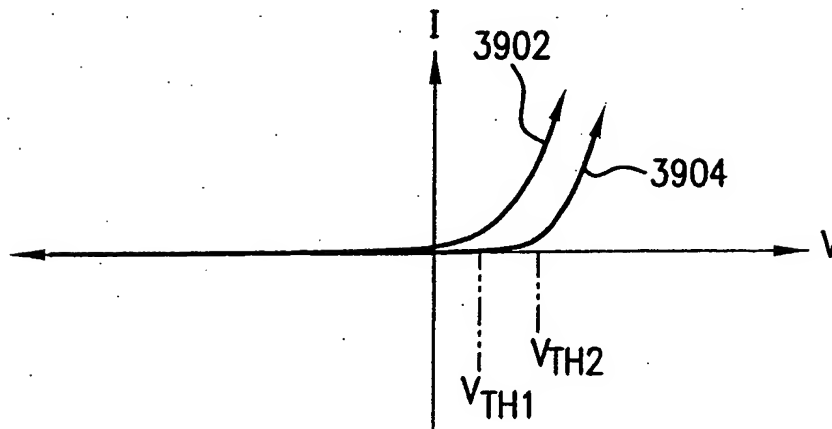


FIG.39

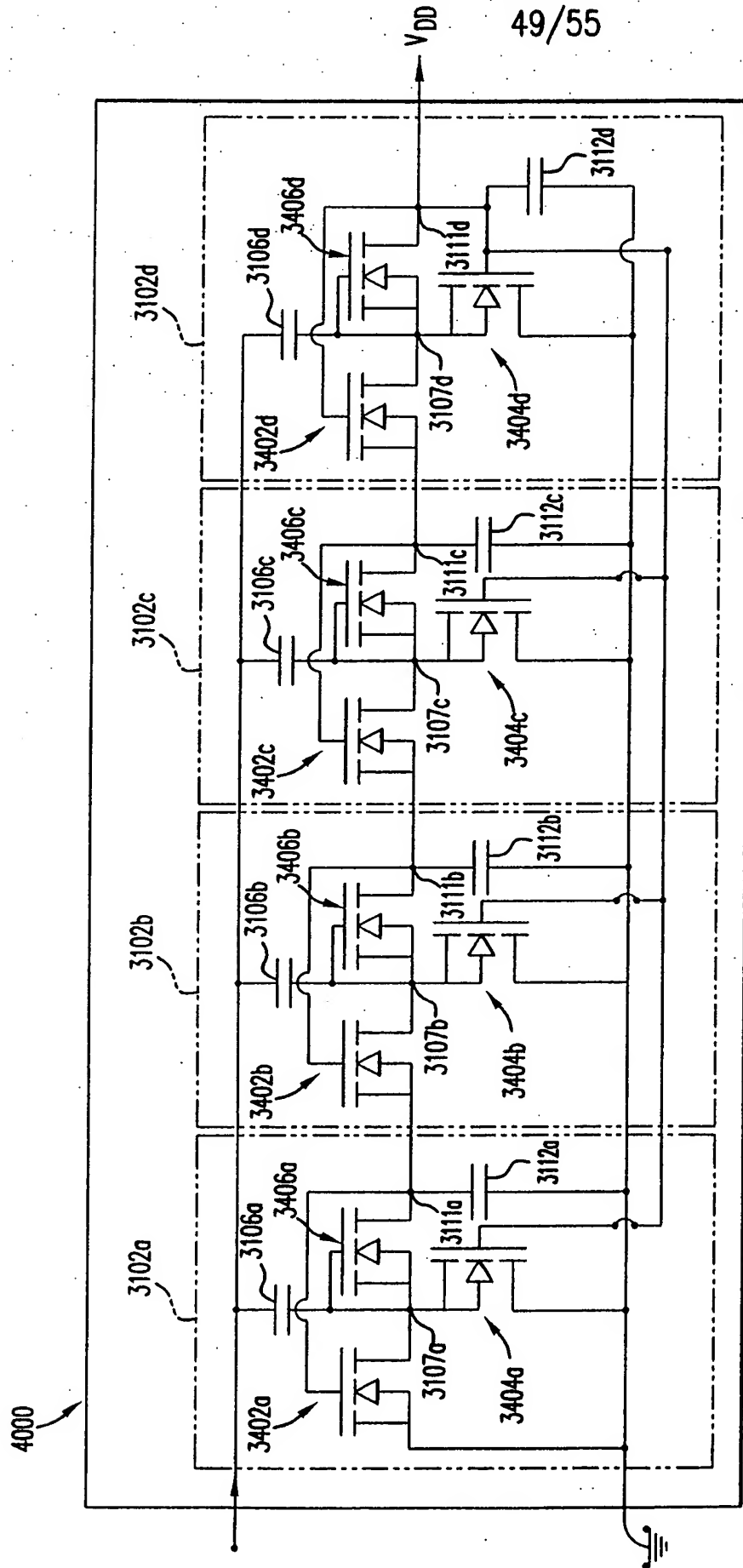


FIG. 40A

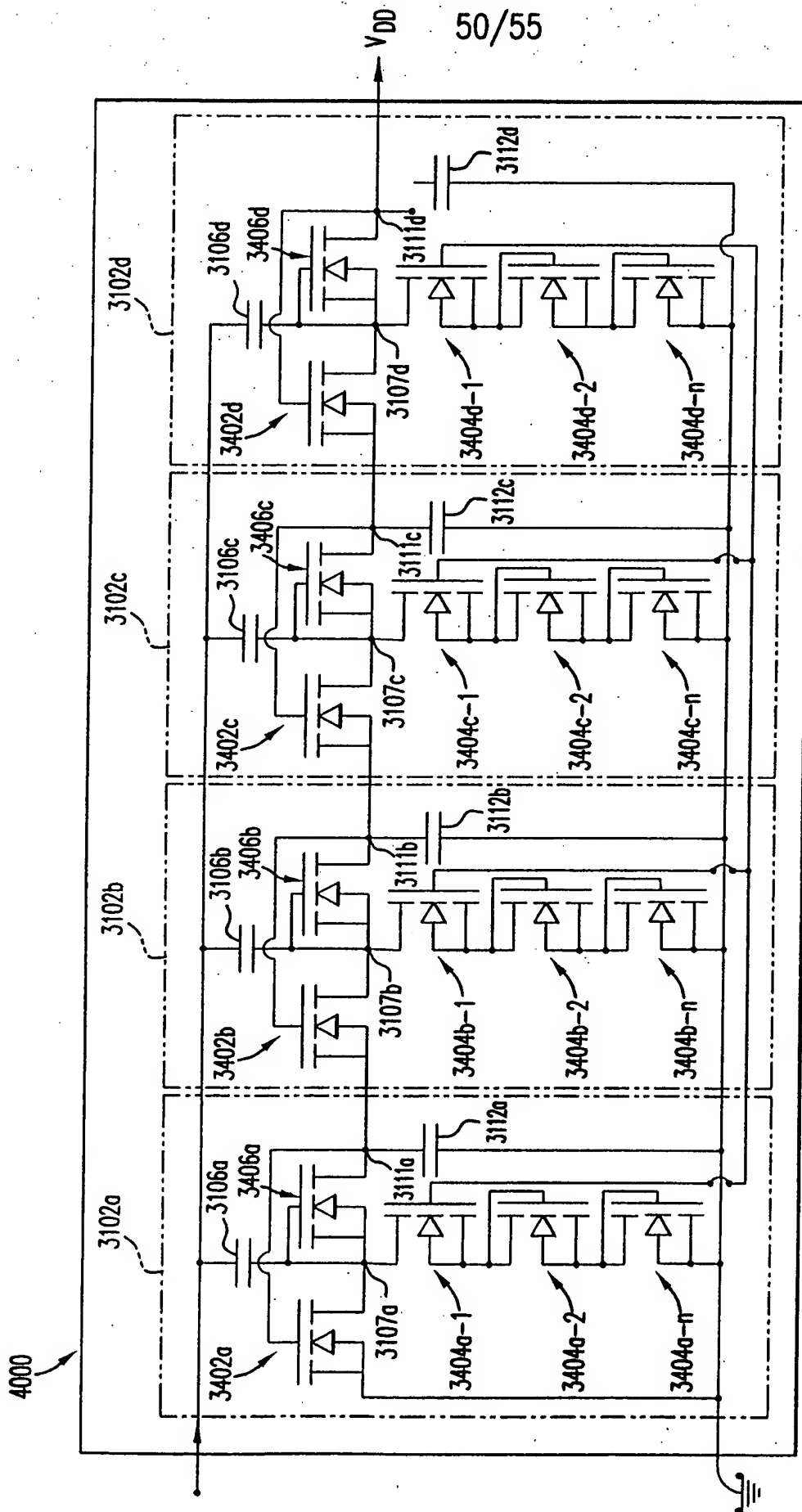


FIG. 40B

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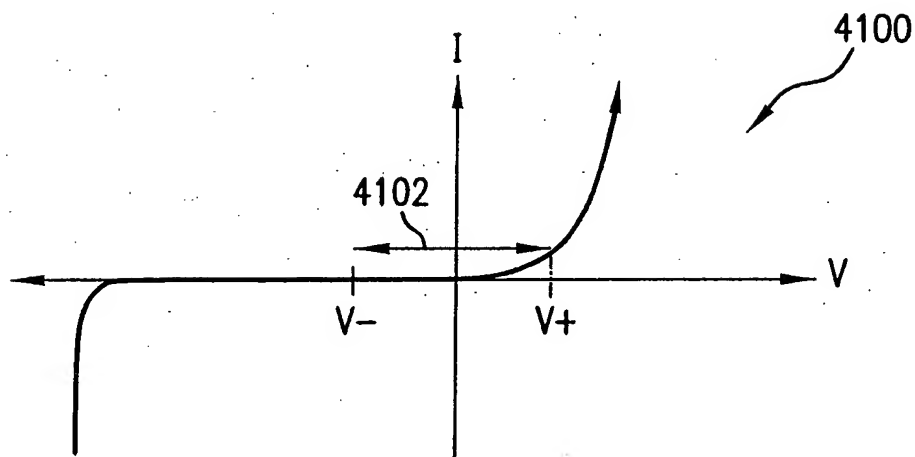


FIG. 41A

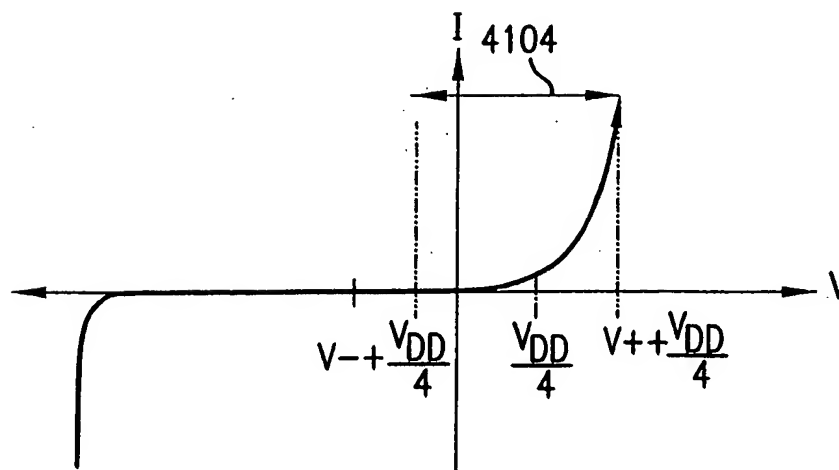


FIG. 41B

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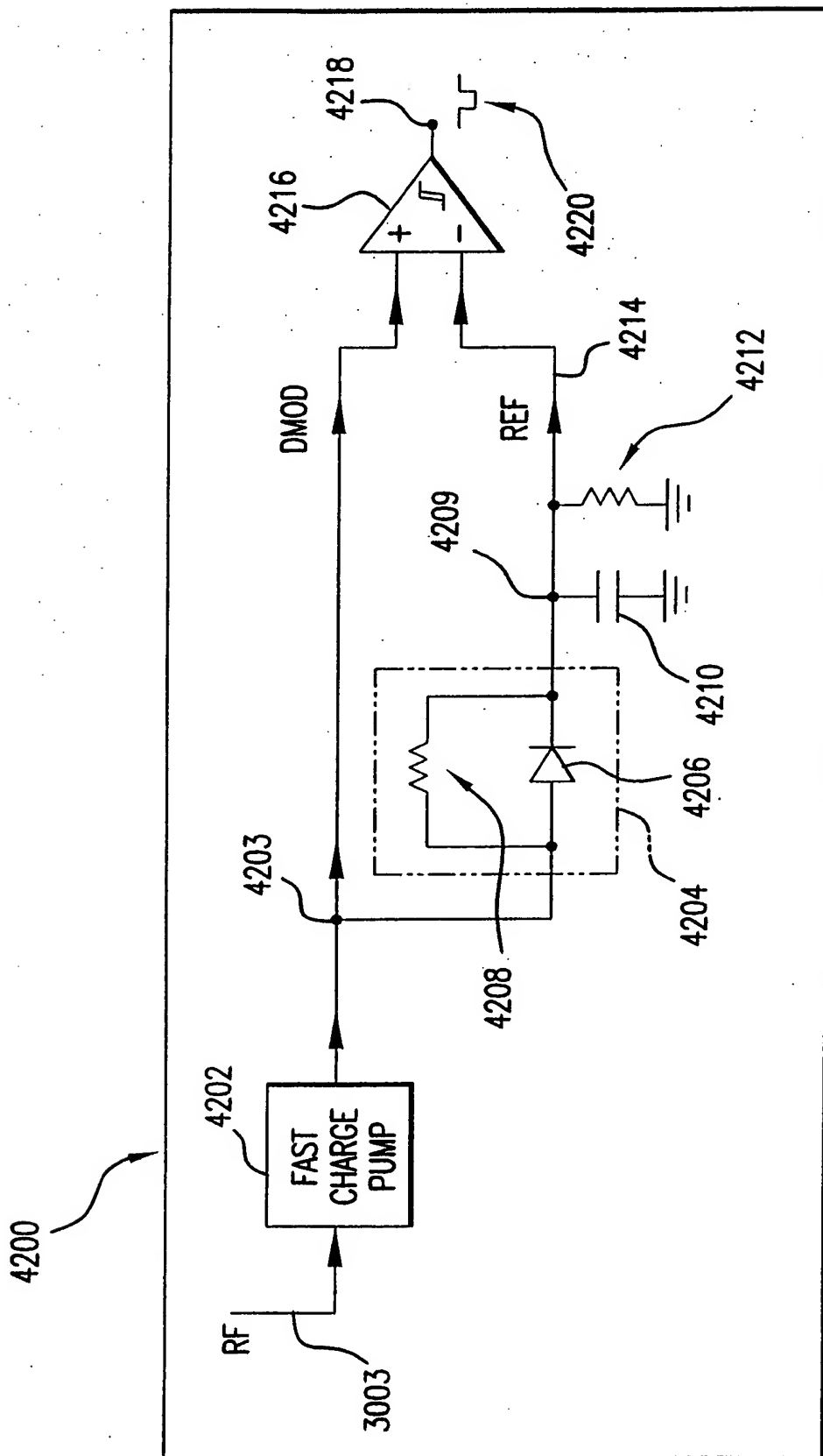


FIG.42

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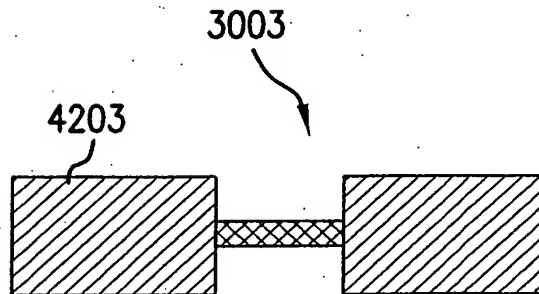


FIG. 43A

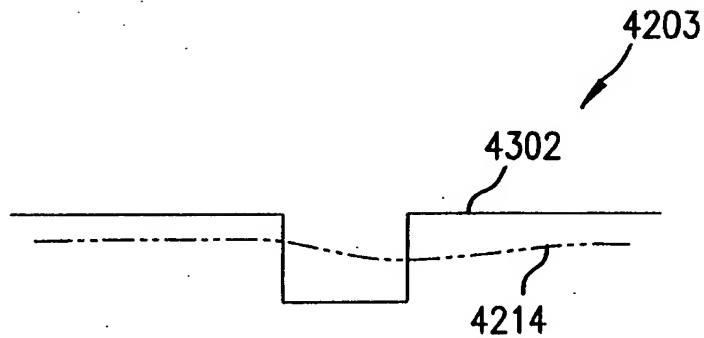


FIG. 43B

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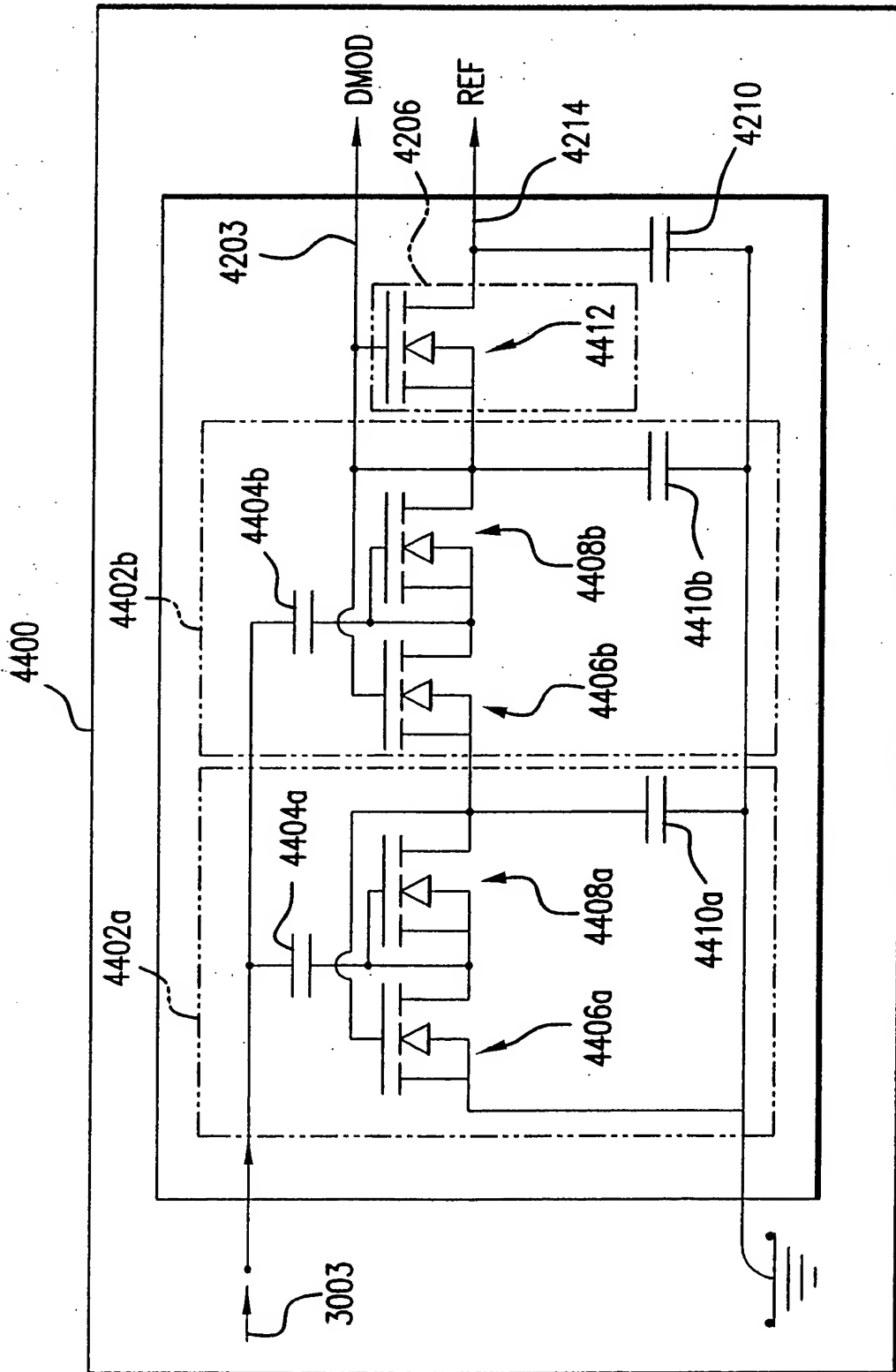


FIG. 44

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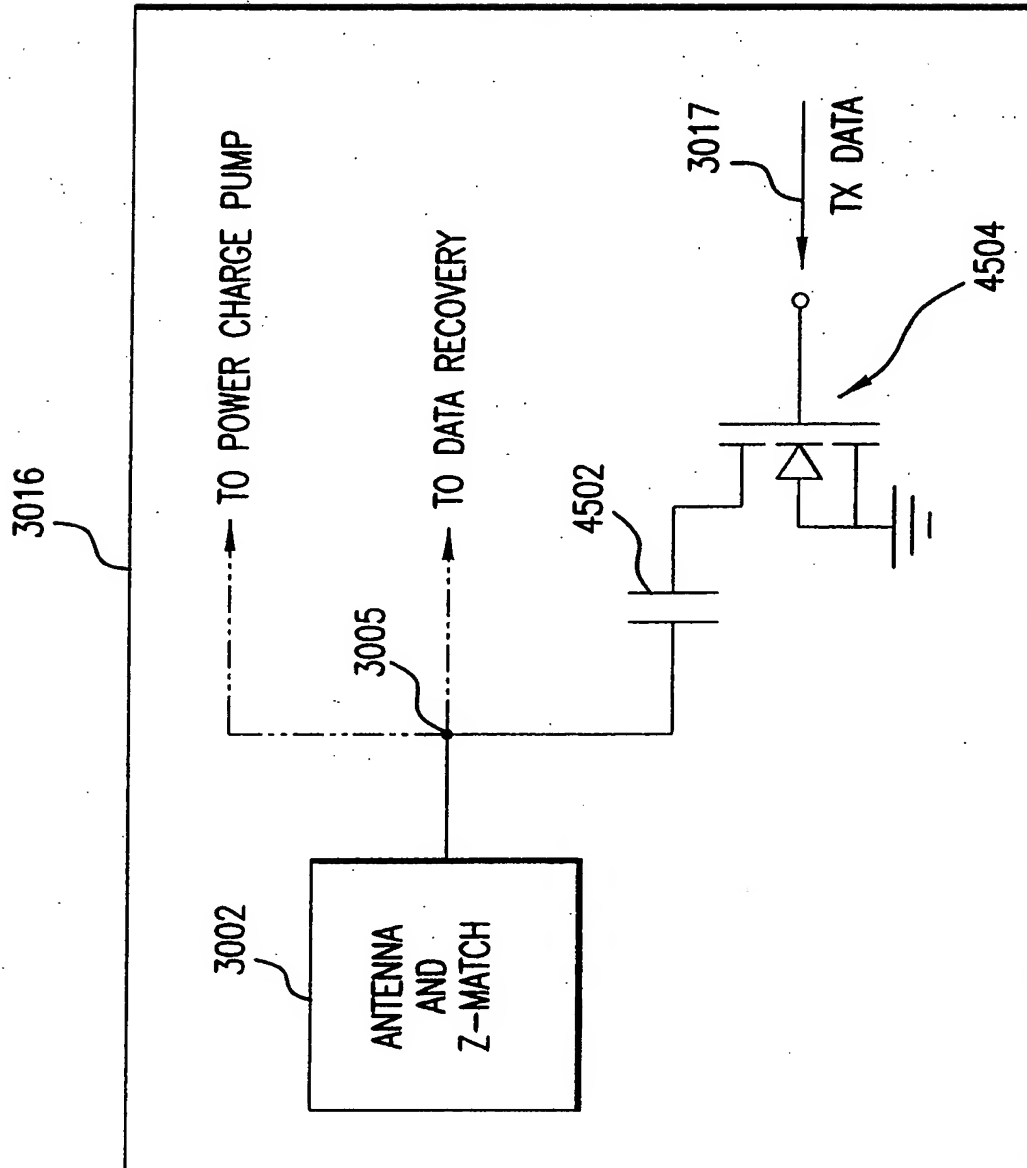


FIG. 45